

**SANYO**

No.1039C

LC7815

**2-Pole 4-Position Analog Function Switch**

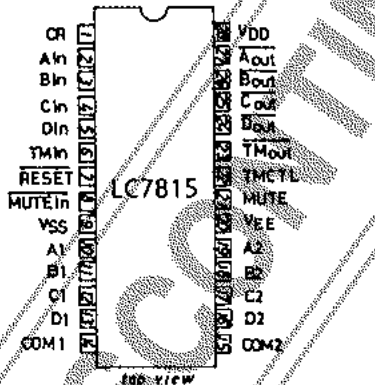
The LC7815 is a 2-pole 4-position analog function switch with 2 built-in C-MOS analog switches (LC4066 type). A soft touch of a button enables switchover of the input signal source of an audio amplifier.

**Use**

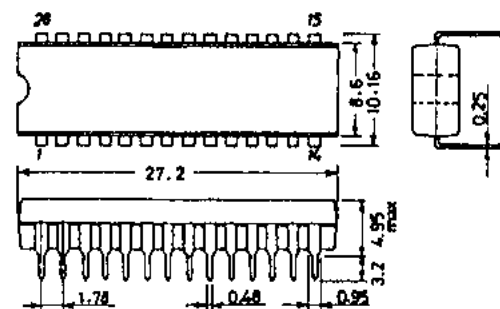
Function switchover of amplifier, receiver, etc. (2 poles 4 positions)

**Features**

1. Good distortion characteristic because of built-in analog switches of LC4066 type. Distortion 0.01 % max./  
 $V_{in} = 1V_{rms}$ ,  $V_{DD} = 15$  to  $18V$
2. Capable of outputting audio muting control signal to minimize noise to be generated at the time of switchover
3. Built-in controller for tape monitor switchover (using LC4066B together)
4. Built-in driver for LED which displays function mode, tape monitor mode
5. Since control input can be operated from + supply alone when using dual supplies, interface with other circuits can be achieved easily.
6. Since audio muting control signal can be triggered independently from external pin ( $MUTE_{in}$ ); audio muting at the time of return from backup can be achieved easily.
7. Control input pin (**RESET**) to be used for turning OFF all analog switches
8. Backup can be performed easily because of C-MOS structure. (Backup voltage: 3 V min.)
9. Operating voltage: 4.5 to 18.0 V/single supply,  $\pm 4.5$  to  $\pm 9.0$  V/dual supplies
10. Package: DIP-28 (Shrink type)

**Pin Assignment**

Case Outline 3029A-D28SIC  
(unit: mm)



SANYO: DIP28S

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

Specifications and information herein are subject to change without notice.

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7128YT/8064KI/4204KI, TS \* No.1039-1/8

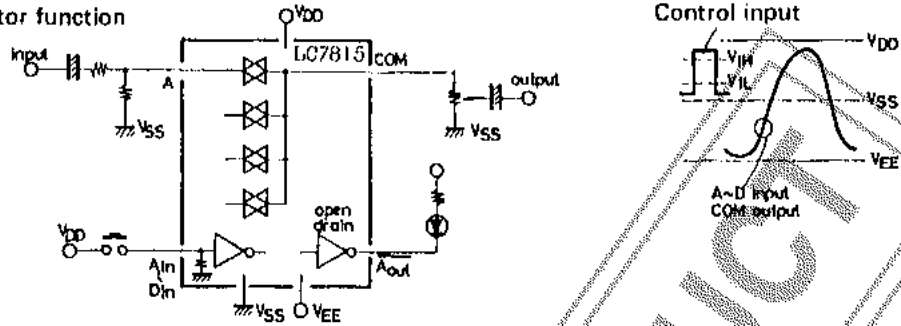


Pin Description

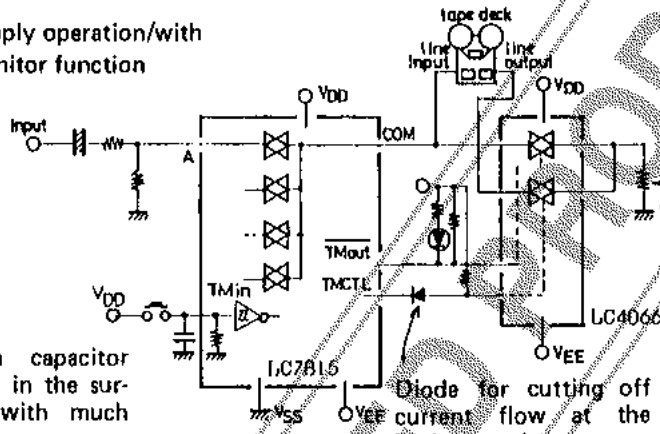
Pin Name	Pin No.	Type of Input/Output	Pin Functions																									
V <sub>DD</sub> V <sub>SS</sub> V <sub>EE</sub>	28 9 20		<ul style="list-style-type: none"> <li>Power supply pins</li> <li>Single supply (+): V<sub>SS</sub>=V<sub>EE</sub>=GND</li> <li>Dual supplies (+-): V<sub>SS</sub>=GND, V<sub>EE</sub>=(-)V</li> </ul>																									
A <sub>in</sub> , B <sub>in</sub> , C <sub>in</sub> , D <sub>in</sub>	2, 3, 4, 5		<ul style="list-style-type: none"> <li>Specified input pins for turning ON individual analog switches</li> <li>Priority order of simultaneous push (A<sub>in</sub> &gt; B<sub>in</sub> &gt; C<sub>in</sub> &gt; D<sub>in</sub>)</li> <li>Prevention of malfunction attributable to pulse noise (Pulse width is discriminated by muting delay time.)</li> </ul>																									
A <sub>out</sub> , B <sub>out</sub> , C <sub>out</sub> , D <sub>out</sub>	27, 26, 25, 24		<ul style="list-style-type: none"> <li>Output of driver for LED which displays ON state corresponding to individual analog switches</li> <li>N channel open drain (Source is connected to V<sub>EE</sub>)</li> </ul>																									
A <sub>1</sub> , B <sub>1</sub> , C <sub>1</sub> , D <sub>1</sub>  A <sub>2</sub> , B <sub>2</sub> , C <sub>2</sub> , D <sub>2</sub>  COM 1 COM 2	10, 11, 12, 13  19, 18, 17, 16  14 15		<ul style="list-style-type: none"> <li>A to D: Audio signal input pins</li> <li>COM: Audio signal output pins</li> <li>Signal inputs (A to D) conduct according to signal inputs (A<sub>in</sub> to D<sub>in</sub>) as follows:</li> </ul> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>COM output</th> <th>A<sub>n</sub></th> <th>B<sub>n</sub></th> <th>C<sub>n</sub></th> <th>D<sub>n</sub></th> </tr> </thead> <tbody> <tr> <td>A<sub>in</sub></td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>B<sub>in</sub></td> <td>*</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>C<sub>in</sub></td> <td>*</td> <td>*</td> <td>1</td> <td>0</td> </tr> <tr> <td>D<sub>in</sub></td> <td>*</td> <td>*</td> <td>*</td> <td>1</td> </tr> </tbody> </table> <p style="text-align: center;">*: Don't care.</p>	COM output	A <sub>n</sub>	B <sub>n</sub>	C <sub>n</sub>	D <sub>n</sub>	A <sub>in</sub>	1	0	0	0	B <sub>in</sub>	*	1	0	0	C <sub>in</sub>	*	*	1	0	D <sub>in</sub>	*	*	*	1
COM output	A <sub>n</sub>	B <sub>n</sub>	C <sub>n</sub>	D <sub>n</sub>																								
A <sub>in</sub>	1	0	0	0																								
B <sub>in</sub>	*	1	0	0																								
C <sub>in</sub>	*	*	1	0																								
D <sub>in</sub>	*	*	*	1																								
TM <sub>in</sub>	6		<ul style="list-style-type: none"> <li>Input pin for specifying tape monitor mode ON/OFF</li> <li>Rise of input signal is detected; monitor mode ON/OFF are inverted to monitor mode OFF/ON respectively.</li> </ul>																									
TMCTL	22		<ul style="list-style-type: none"> <li>Output pin for controlling external analog switch (LC4066B) for tape monitor</li> <li>Source of N channel transistor of complementary buffer output is connected to V<sub>EE</sub>.</li> </ul>																									
TM <sub>out</sub>	23		<ul style="list-style-type: none"> <li>Output pin for driver for LED which displays tape monitor state as well as external analog switch (LC4066B) for tape monitor</li> <li>TM<sub>out</sub> is opposite in polarity to TMCTL.</li> </ul>																									
MUTE <sub>in</sub>	8		<ul style="list-style-type: none"> <li>Input pin for forcing audio muting control signal (MUTE) to be triggered externally</li> <li>If fixed at 'L' level, MUTE output becomes 'H' level.</li> </ul>																									
MUTE	21		<ul style="list-style-type: none"> <li>Output pin for audio muting control signal</li> <li>Signal with pulse width to be determined by external constant at CR pin is output at the time of function switchover or MUTE<sub>in</sub> input.</li> </ul>																									
CR	1		<ul style="list-style-type: none"> <li>CR time constant pin for determining time interval of audio muting control signal</li> <li>Time lag (muting delay) between muting signal rise and analog switch switchover depends on C·R<sub>S</sub> time constant at the time of transistor ON.</li> </ul>																									
RESET	7		<ul style="list-style-type: none"> <li>Input pin for turning OFF all analog switches and resetting tape monitor flip-flop ('L' level active)</li> </ul>																									

■ Sample Application Circuits

1. Dual-supply operation/without tape monitor function



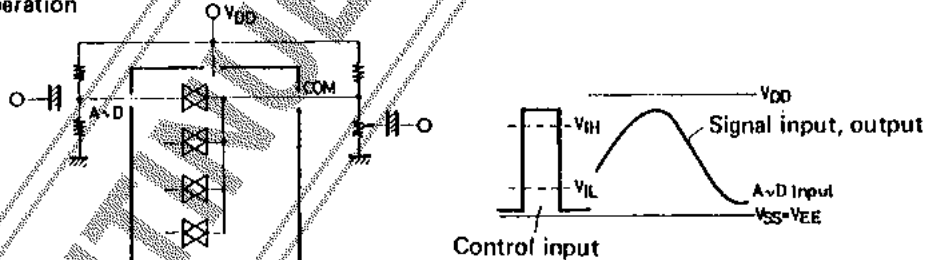
2. Dual-supply operation/with tape monitor function



Connect a capacitor when using in the surroundings with much noise.

Diode for cutting off current flow at the backup mode.

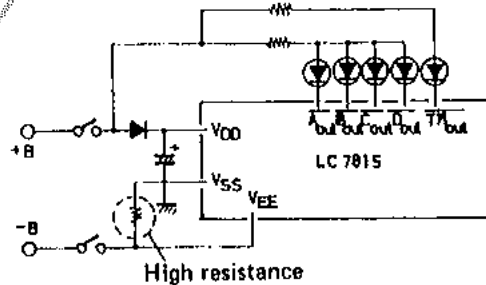
3. Single-supply operation



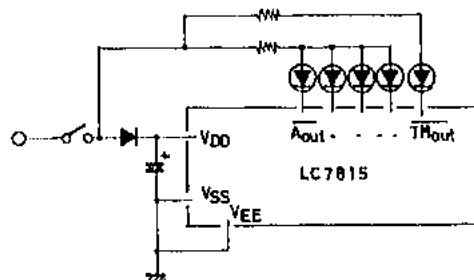
For using tape monitor function, make connection as shown in 2 above.

4. Backup

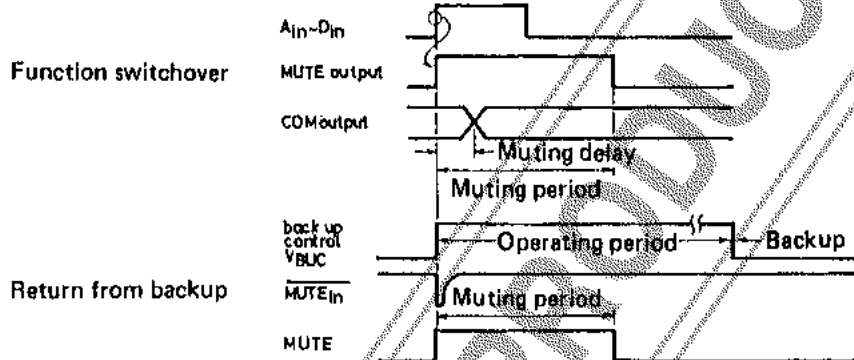
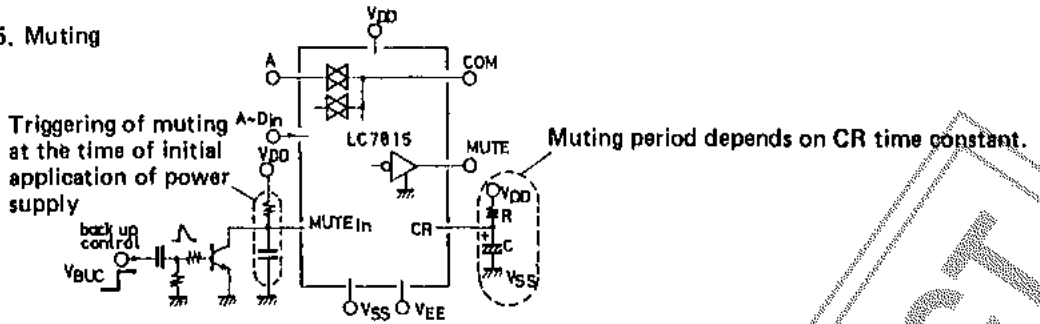
(1) Dual-supply operation



(2) Single-supply operation



5. Muting



Absolute Maximum Ratings/ $T_a=25 \pm 2^\circ\text{C}$

Parameter	Symbol	Conditions	Unit
Maximum Supply Voltage	$V_{DD \text{ max}}$	$V_{SS}-0.3 \sim V_{EE}+20$	V
	$V_{EE \text{ max}}$	$V_{DD}-20 \sim V_{SS}+0.3$	V
Output Current	$I_{OUT}$	$A_{out}, B_{out}, C_{out}, D_{out}, TM_{out}$	30 mA
Output Voltage	$V_{OUT}$	$A_{out}, B_{out}, C_{out}, D_{out}, TM_{out}$	$V_{EE}-0.3 \sim V_{DD}+0.3$ V
Voltage Difference at Analog Switch ON	$\Delta V_{on}$	Switch ON	0.5 V
Allowable Power Dissipation	$P_{d \text{ max}}$	$T_a \leq 85^\circ\text{C}$	350 mW
Operating Temperature	$T_{opg}$		$-40 \sim +85$ °C
Storage Temperature	$T_{stg}$		$-40 \sim +125$ °C

Allowable Operating Conditions/ $T_a = -40 \sim +85^\circ\text{C}$

Characteristic	Symbol	Pin No.	Conditions	min	typ	max	unit
Supply Voltage	$V_{DD1}$	$V_{DD}(28)$	$V_{EE} \leq V_{SS}$	$V_{SS}+4.5$		$V_{EE}+18$	V
	$V_{EE}$	$V_{EE}(20)$	$V_{DD} \geq V_{SS}+4.5$	$V_{DD}-18$		$V_{SS}$	V
	$V_{DD2}$	$V_{DD}(28)$	Backup, $V_{EE} \leq V_{SS}$	$V_{SS}+3$		$V_{SS}+18$	V
'H' Level Input Voltage	$V_{IH1}$	$A_{in}(2) \sim D_{in}(5),$ $RESET(7), MUTE_{in}(8)$		$0.75V_{DD}$		$V_{DD}$	V
	$V_{IH2}$	$TM_{in}(6)$		$0.8V_{DD}$		$V_{DD}$	V
'L' Level Input Voltage	$V_{IL1}$	$A_{in}(2) \sim D_{in}(5),$ $RESET(7), MUTE_{in}(8)$		$V_{SS}$		$0.25V_{DD}$	V
	$V_{IL2}$	$TM_{in}(6)$		$V_{SS}$		$0.2V_{DD}$	V
Analog Switch Input Voltage	$V_{IN}$	$A_1(10) \sim D_1(13),$ $A_2(19) \sim D_2(16)$		$V_{EE}$		$V_{DD}$	V
External Capacitance for Muting Timer	C	CR(1)				10	$\mu\text{F}$
External Resistance for Muting Timer	R	CR(1)	$V_{DD}-V_{SS}=4.5\text{V}$	40		100	$\text{k}\Omega$
			$V_{DD}-V_{SS} \geq 9\text{V}$	100		300	$\text{k}\Omega$
Input Receiving Pulse Width	$T_{IN}$	$A_{in}(2) \sim D_{in}(5),$ $TM_{in}(6)$	$V_{DD}=9\text{V}, C=3.3\mu\text{F},$ $R=220\text{k}\Omega$	120			ms

Electrical Characteristics/Ta=25 ±2°C, VSS=0V

Characteristic	Symbol	Pin No.	Conditions	min	typ	max	unit
'H' Level Output Voltage	VOH1	TMCTL(22)	I <sub>OH</sub> =-0.1mA V <sub>DD</sub> =4.5~18V	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
	VOH2	MUTE(21)	I <sub>OH</sub> =-0.4mA, V <sub>DD</sub> =4.5V	V <sub>DD</sub> -1.5		V <sub>DD</sub>	V
			I <sub>OH</sub> =-0.4mA, V <sub>DD</sub> =9V	V <sub>DD</sub> -0.5		V <sub>DD</sub>	V
'L' Level Output Voltage	VOL1	TMCTL(22)	I <sub>OL</sub> =0.1mA	V <sub>EE</sub>		0.2X (V <sub>DD</sub> -V <sub>EE</sub> )	V
	VOL2	MUTE(21)	I <sub>OL</sub> =0.4mA, V <sub>DD</sub> =4.5V	0		1.5	V
			I <sub>OL</sub> =0.4mA, V <sub>DD</sub> =9V	0		0.5	V
	VOL3	A <sub>out</sub> (27) to D <sub>out</sub> (24), TM <sub>out</sub> (23)	I <sub>OL</sub> =7mA, V <sub>DD</sub> -V <sub>EE</sub> =4.5V	V <sub>EE</sub>		V <sub>EE</sub> +2	V
			I <sub>OL</sub> =30mA, V <sub>DD</sub> -V <sub>EE</sub> =9V	V <sub>EE</sub>		V <sub>EE</sub> +4	V
Analog Switch ON Resistance	R <sub>on</sub>	A <sub>1</sub> (10), B <sub>1</sub> (11), C <sub>1</sub> (12), D <sub>1</sub> (13), COM1(14), A <sub>2</sub> (19), B <sub>2</sub> (18), C <sub>2</sub> (17), D <sub>2</sub> (16), COM2(15)	I=1mA, V <sub>DD</sub> -V <sub>EE</sub> =4.5V		400		Ω
			I=1mA, V <sub>DD</sub> -V <sub>EE</sub> =9V		120		Ω
			I=1mA, V <sub>DD</sub> -V <sub>EE</sub> =18V		80		Ω
'H' Level Input Current	I <sub>IH1</sub>	A <sub>in</sub> (2), B <sub>in</sub> (3), C <sub>in</sub> (4), D <sub>in</sub> (5), TM <sub>in</sub> (6)	V <sub>DD</sub> =9V, V <sub>IN</sub> =V <sub>DD</sub>	20		90	μA
	I <sub>IH2</sub>	MUTE <sub>in</sub> (8)	V <sub>IN</sub> =V <sub>DD</sub> =18V			10	μA
'L' Level Input Current	I <sub>IL1</sub>	RESET(7)	V <sub>DD</sub> =9V, V <sub>IN</sub> =V <sub>DD</sub>	-90		-20	μA
	I <sub>IL2</sub>	MUTE <sub>in</sub> (8)	V <sub>IN</sub> =V <sub>SS</sub>	-10			μA
Input/Output OFF Leak Current	I <sub>OFF1</sub>	A <sub>out</sub> (27)~D <sub>out</sub> (24), TM <sub>out</sub> (23)	Output transistor OFF V <sub>O</sub> =V <sub>EE</sub> +18V			10	μA
	I <sub>OFF2</sub>	CR(1)	Output transistor OFF V <sub>O</sub> =V <sub>SS</sub> +18V			3	μA
	I <sub>OFF3</sub>	A <sub>1</sub> (10),~D <sub>1</sub> (13), COM1(14), A <sub>2</sub> (19)~D <sub>2</sub> (16), COM2(15)	Analog switch OFF V <sub>IN</sub> =V <sub>O</sub> =V <sub>EE</sub> to 18V	-10		10	μA
Input Floating Voltage	V <sub>IF1</sub>	A <sub>in</sub> (2)~D <sub>in</sub> (5), TM <sub>in</sub> (6)	V <sub>DD</sub> =4.5 to 18V			0.75	V
	V <sub>IF2</sub>	RESET(7)	V <sub>DD</sub> =4.5 to 18V		V <sub>DD</sub> -0.75		V
Total Harmonic Distortion	THD1	COM1(14), COM2(15)	V <sub>IN</sub> =1V <sub>rms</sub> , f=1kHz, V <sub>DD</sub> -V <sub>EE</sub> =15 to 18V, Refer to Fig. 1.			0.01	%
	THD2	COM1(14), COM2(15)	V <sub>IN</sub> =0.1V <sub>rms</sub> , f=1kHz, V <sub>DD</sub> -V <sub>EE</sub> =4.5V, Refer to Fig. 1.			0.05	%
Feedthrough (Switch OFF)	FTH	A <sub>1</sub> (10) to COM1(14), D <sub>1</sub> (13) A <sub>2</sub> (19) to COM2(15), D <sub>2</sub> (16)	V <sub>DD</sub> -V <sub>EE</sub> =18V, f=10kHz, V <sub>in</sub> =0.77V <sub>rms</sub> , Refer to Fig. 2. R <sub>L</sub> =47kΩ		55		dB
Crosstalk	CT	A <sub>1</sub> (10) to COM2(15), D <sub>1</sub> (13) A <sub>2</sub> (19) to COM1(14), D <sub>2</sub> (16)	V <sub>DD</sub> -V <sub>EE</sub> =18V, f=10kHz, V <sub>in</sub> =0.77V <sub>rms</sub> , Refer to Fig. 3. R <sub>L</sub> =47kΩ		75		dB
Muting period	TM1	MUTE(21)	V <sub>DD</sub> =9V, Refer to Fig. 4. C=3.3μF ±20%, R=220kΩ ±5%	350	580	1000	ms
	TM2	MUTE(21)	V <sub>DD</sub> =9V, C=3.3μF ±0%, R=220kΩ ±0%	450	580	800	ms

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				min	typ	max	unit
Switch Switchover Delay Time	T <sub>SWD</sub>	A <sub>in</sub> (2) to D <sub>in</sub> (5), T <sub>M</sub> <sub>in</sub> (6)	V <sub>DD</sub> =9V, Refer to Fig. 5. C=3.3μF, R=220kΩ	30	50	120	ms
Supply Current	I <sub>DD1</sub>	V <sub>DD</sub> (28)	Operating, Refer to Fig. 6. V <sub>DD</sub> -V <sub>EE</sub> =18V			1000	μA
	I <sub>DD2</sub>	V <sub>DD</sub> (28)	Backup, V <sub>DD</sub> =5V, V <sub>SS</sub> =V <sub>EE</sub>			3	μA

Fig. 1 Total harmonic distortion

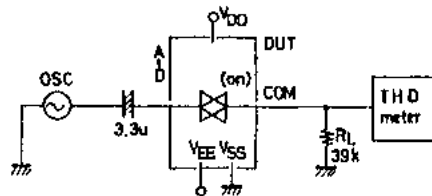


Fig. 2 Feedthrough

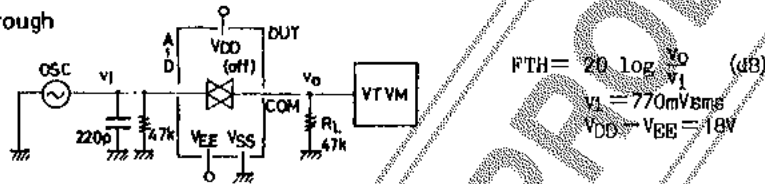


Fig. 3 Crosstalk

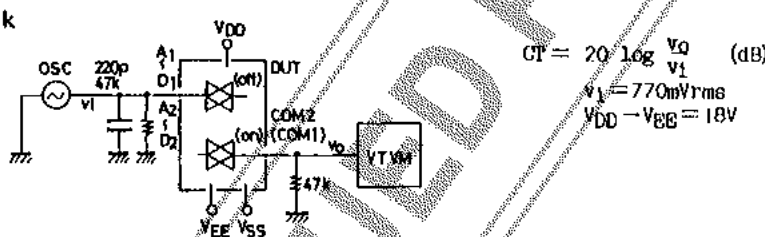


Fig. 4 Muting period

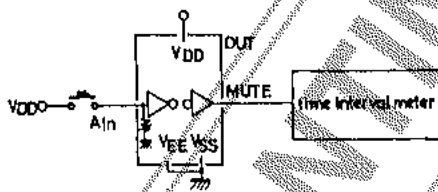


Fig. 6 Supply current

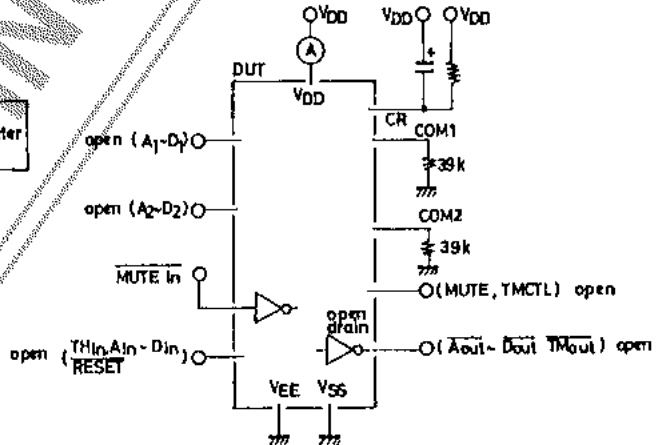
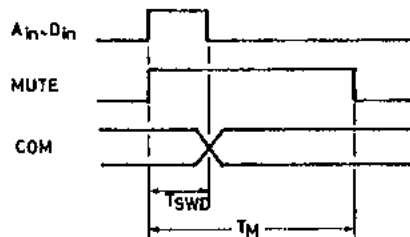
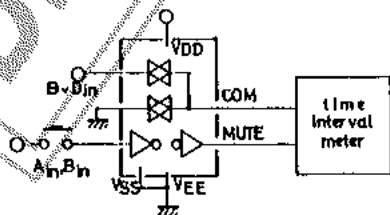
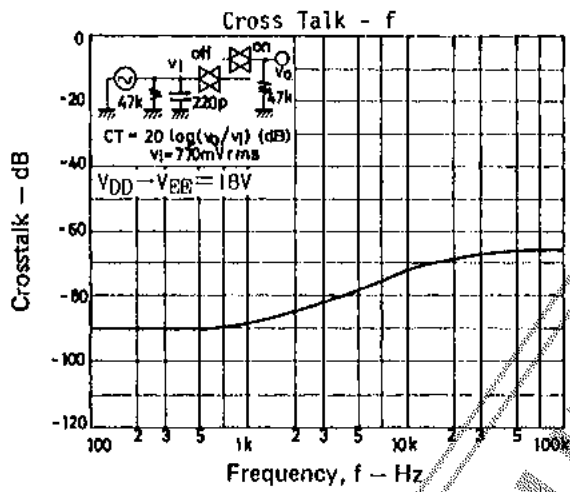
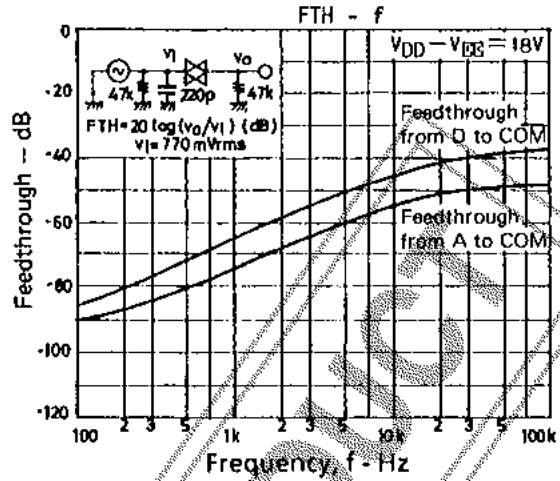
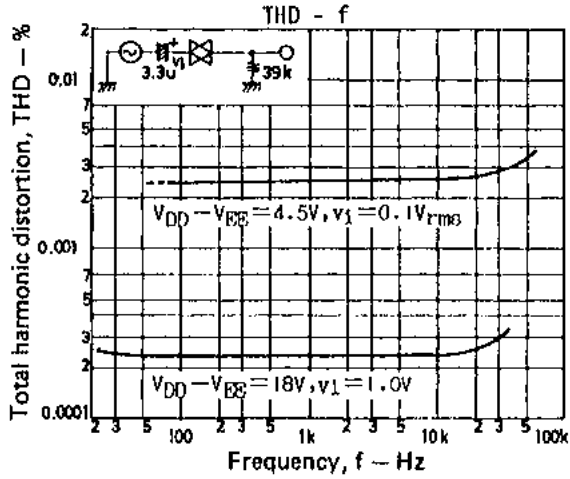


Fig. 5 Switch switchover delay time



T<sub>M</sub>: Muting period  
T<sub>SW</sub>: Switch switchover delay time



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