NEC

MOS Field Effect Power Transistors

2SK2723

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

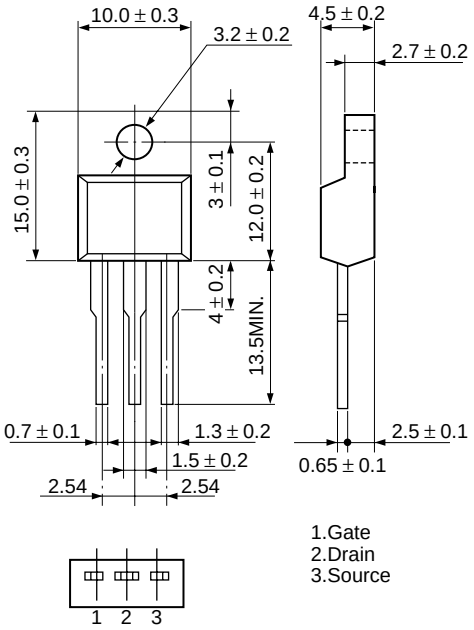
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching spplications.

FEATURES

- Low On-Resistance
  $R_{DS(on)1}$ = 40mΩ Max. (V_{GS} = 10 V, I_D = 13 A)
  $R_{DS(on)2}$ = 60mΩ Max. (V_{GS} = 4 V, I_D = 13 A)
- Low C_{iss} C_{iss} = 830 pF Typ.
- Built-in G-S Protection Diode
- Isolated TO-220 Package

PACKAGE DIMENSIONS
(in millimeter)

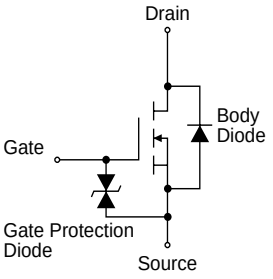


MP-45F (ISOLATED TO-220)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±25	A
Drain Current (pulse)*	$I_{D(pulse)}$	±100	A
Total Power Dissipation (T_A = 25 °C)	P_T	2.0	W
Total Power Dissipation (T_c = 25 °C)	P_T	25	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

*PW ≤ 10 μs, Duty Cycle ≤ 1%



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this deveice acutally used, an addtional protection circiut is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

Document No. D10623EJ2V0DS00 (2nd edition)
Date Published April 1996 P
Printed in Japan

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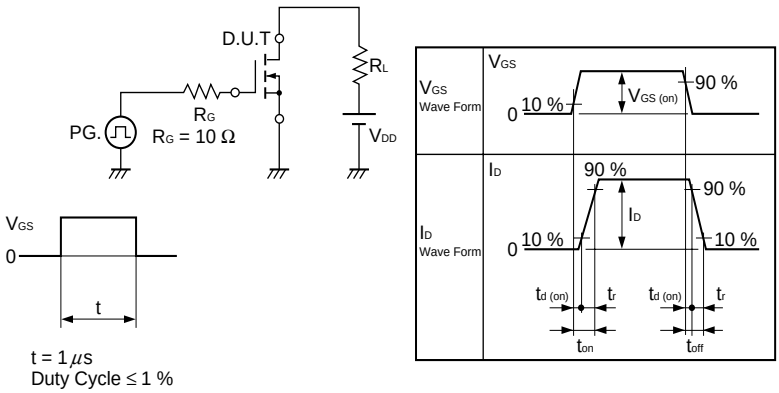
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

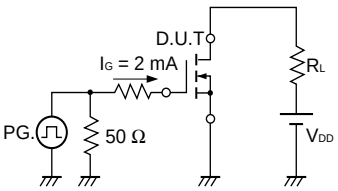
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 13 A		28	40	mΩ
On-state Resistance	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 13 A		45	60	mΩ
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 13 A	8.0	18		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		830		pF
Output Capacitance	C_{oss}	V_{GS} = 0		430		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		185		pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 13 A		21		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		185		ns
Turn-Off Delay Time	$t_{d(off)}$	V_{DD} = 30 V		100		ns
Fall Time	t_f	R_G = 10 Ω		110		ns
Total Gate Charge	Q_G	I_D = 25 A		35		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 48 V		2.8		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		15		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 25 A, V_{GS} = 0		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 25 A, V_{GS} = 0		60		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		125		nC

Test Circuit 1 Switching Time

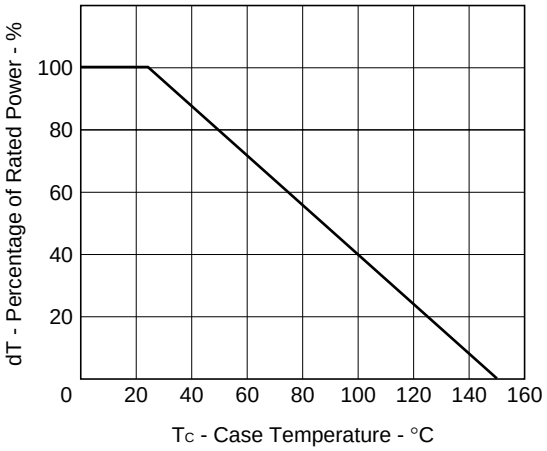


t = 1 μs
Duty Cycle ≤ 1 %

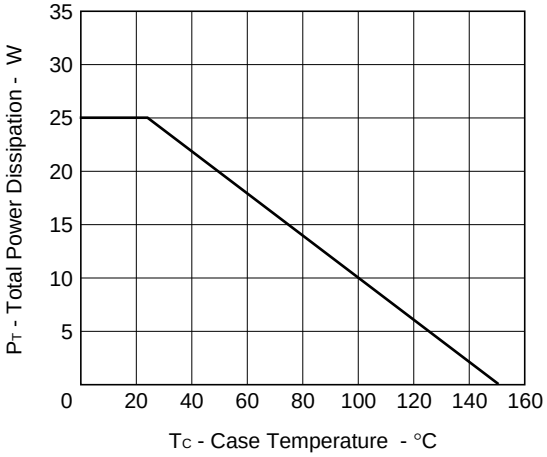
Test Circuit 2 Gate Charge



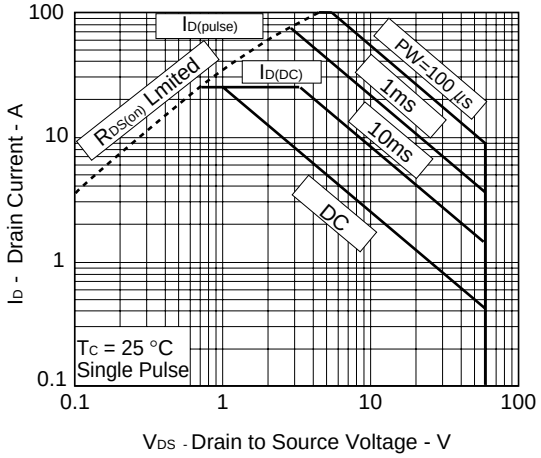
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



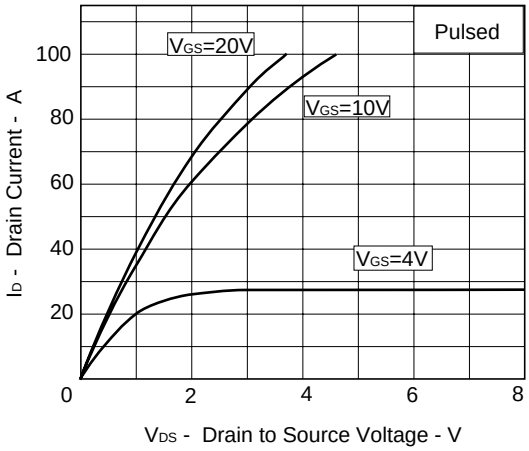
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



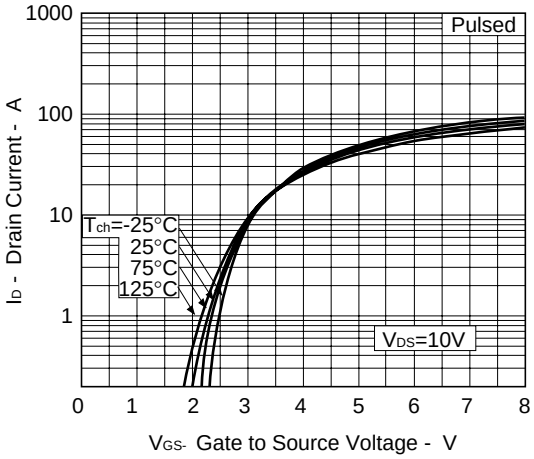
FORWARD BIAS SAFE OPERATING AREA



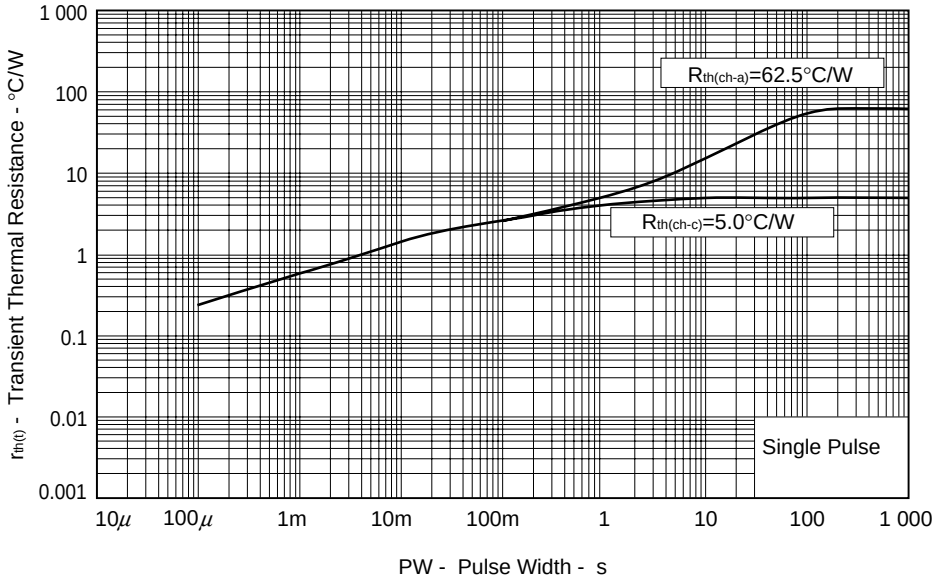
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



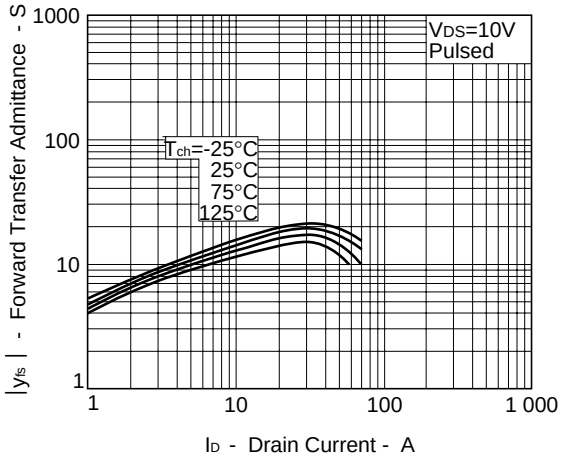
FORWARD TRANSFER CHARACTERISTICS



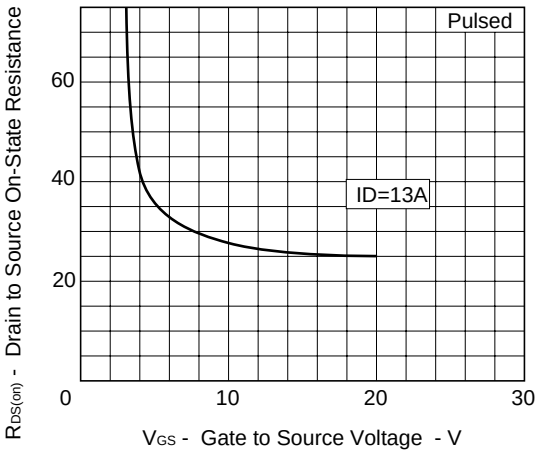
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



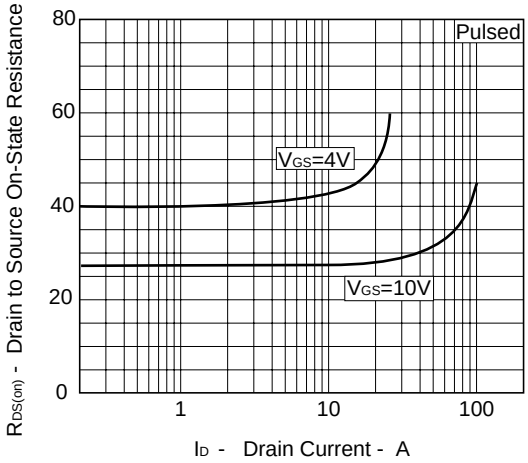
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



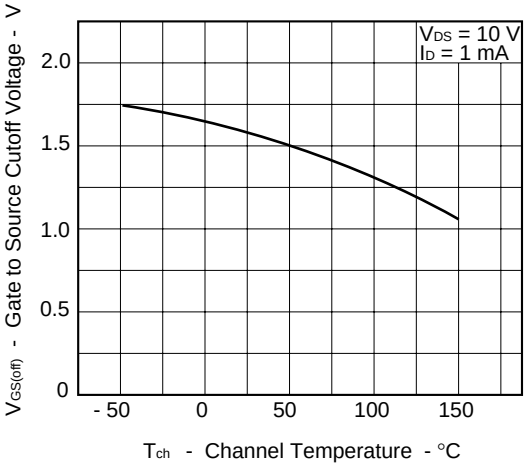
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



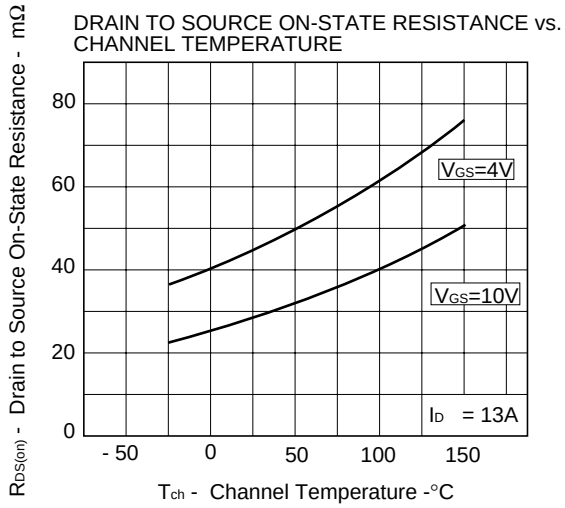
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



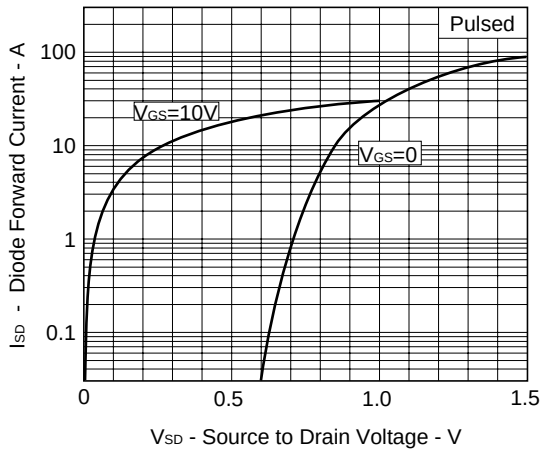
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



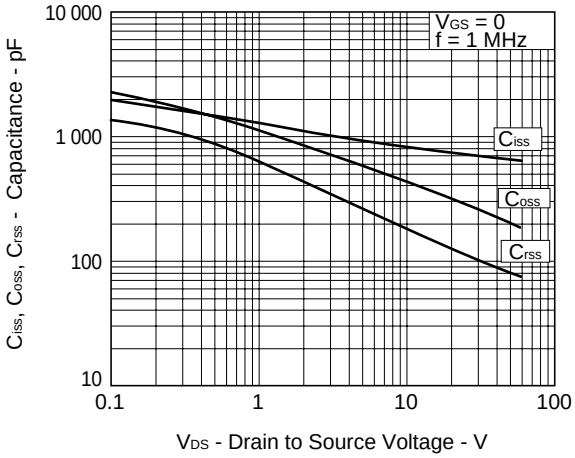
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



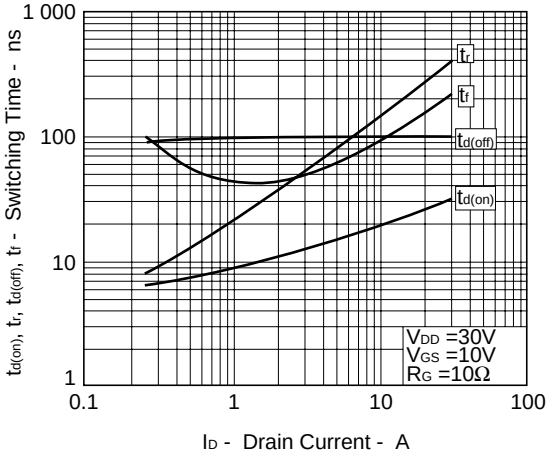
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



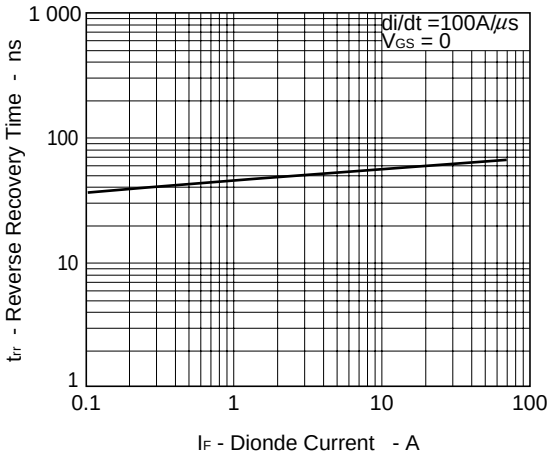
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



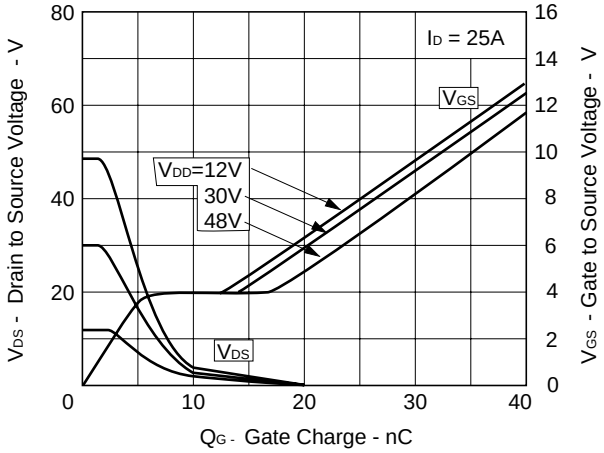
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	C10535E
Semiconductor device package manual.	C10943X
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	X10679E
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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