DATA SHEET

TDA8591J

4 × 44 W into 4 Ω or 4 × 75 W into 2 Ω quad BTL car radio power amplifier

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

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4 × 44 W into 4 Ω or 4 × 75 W into 2 Ω quad BTL car radio power amplifier

TDA8591J

1 FEATURES

- Low quiescent current
- Low distortion
- Low output offset voltage
- Soft thermal clipping to prevent audio holes
- External mute timer for low start-up plop (also allows a fast mute function)
- High output power
- Operating, mute and standby mode selection by two-pin or single-pin operation
- Diagnostic information available:
  - Dynamic Distortion Detection (DDD)
  - High temperature detection
  - Short-circuit detection
  - Detection of output offset due to leakage current at the input
- No switch-on/switch-off plops when switching between standby and mute modes or between mute and operating modes
- Fast mute with supply voltage drops
- Package with flexible leads
- All outputs can withstand short-circuits to ground, to the positive supply voltage and across the load
- Pin CP can withstand short-circuits to its adjacent pins, all other pins can withstand short-circuits to ground and to the positive supply voltage
- ESD protection on all pins
- Thermal protection against junction temperatures exceeding 150 °C
- Load dump protection
- Protected against open ground pins (loss of ground) and outputs short-circuited to supply ground
- All negative outputs are protected against open supply voltage and output short-circuited to supply voltage
- Reverse-polarity safe.

2 GENERAL DESCRIPTION

The TDA8591J is a quad BTL audio power amplifier comprising four independent amplifiers in Bridge Tied Load (BTL) configuration. Each amplifier has a gain of 26 dB and supplies an output power of 75 W (EIAJ) into a 2 Ω load. The TDA8591J has low quiescent current and is primarily developed for car audio applications.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8591J	DBS27P	plastic DIL-bent-SIL power package; 27 leads (lead length 7.7 mm)	SOT521-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		8.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current		120	200	290	mA
I_{stb}	standby supply current		–	2	50	μA
$\lvert Z_i \rvert$	input impedance		–	70	–	kΩ
P_o	output power	THD + N = 0.5%				
		R_L = 4 Ω	19	22	–	W
		R_L = 2 Ω	–	34	–	W
		THD + N = 10%				
		R_L = 4 Ω	27	28	–	W
		R_L = 2 Ω	–	47	–	W
		EAIJ values				
		R_L = 4 Ω	41.5	44	–	W
		R_L = 2 Ω	–	75	–	W
$\lvert V_{OO} \rvert$	output offset voltage	mute mode	–	–	30	mV
		DC operating mode	–	–	60	mV
G_v	voltage gain	V_i = 40 mV (RMS)	25	26	27	dB
THD + N	total harmonic distortion plus noise	P_o = 1 W; f = 1 kHz; R_L = 4 Ω	–	0.03	0.1	%
α_{cs}	channel separation	V_i = 40 mV (RMS); R_s = 0 Ω	56	68	–	dB
$V_{n(o)}$	noise output voltage	R_s = 0 Ω; see Fig.29	–	70	–	μV
SVRR	supply voltage ripple rejection	V_{ripple} = 2 V (p-p); mute or operating mode; R_s = 0 Ω; see Fig.29	54	68	–	dB

5 BLOCK DIAGRAM

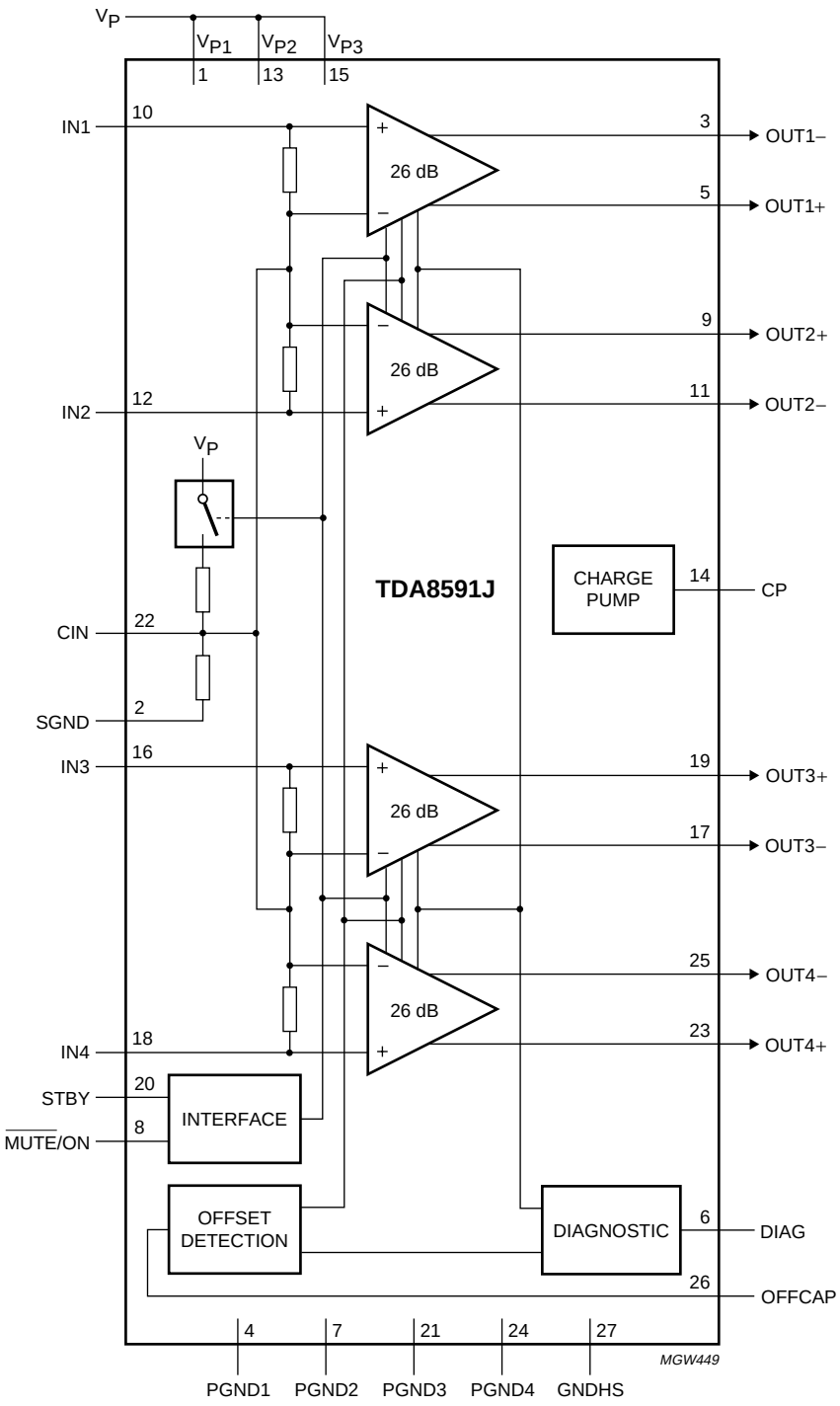


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	power supply to channels 1 and 4
SGND	2	signal ground
OUT1–	3	channel 1 negative output
PGND1	4	channel 1 power ground
OUT1+	5	channel 1 positive output
DIAG	6	diagnostic output
PGND2	7	channel 2 power ground
$\overline{\text{MUTE}}$/ON	8	mode select input: mute/amplifier operating (via mute timer)
OUT2+	9	channel 2 positive output
IN1	10	channel 1 input
OUT2–	11	channel 2 negative output
IN2	12	channel 2 input
V_{P2}	13	channel 2 power supply
CP	14	charge pump capacitor
V_{P3}	15	channel 3 power supply
IN3	16	channel 3 input
OUT3–	17	channel 3 negative output
IN4	18	channel 4 input
OUT3+	19	channel 3 positive output
STBY	20	standby select input
PGND3	21	channel 3 power ground
CIN	22	common input voltage
OUT4+	23	channel 4 positive output
PGND4	24	channel 4 power ground
OUT4–	25	channel 4 negative output
OFFCAP	26	offset detection capacitor
GNDHS	27	ground (heatsink of encapsulation)

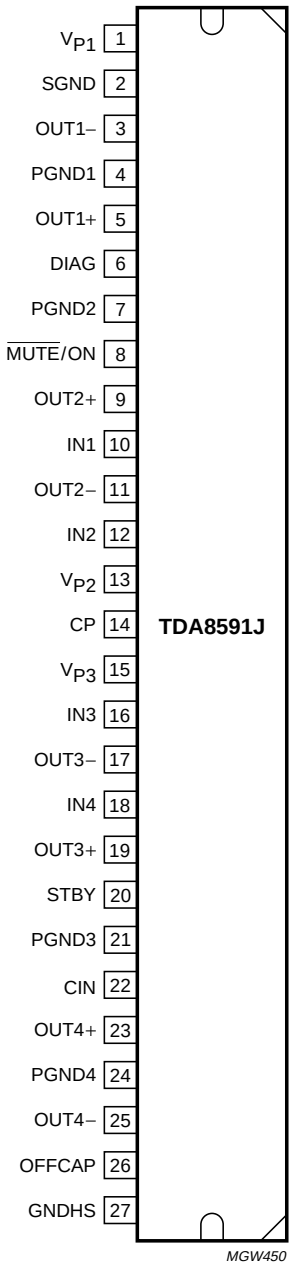


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The TDA8591J is an audio power amplifier with four independent Bridge Tied Load (BTL) amplifiers with high output power and low distortion. The gain of each amplifier is fixed at 26 dB. The TDA8591J has two-pin mode control which allows the amplifiers to be switched to standby (off) with the STBY pin, and the $\overline{\text{MUTE}}$/ON pin to be used to switch between mute mode (input signal suppressed) and amplifier operating mode.

Special attention is paid to dynamic behaviour:

- A fast mute that switches all amplifiers to mute mode at low supply voltage and suppresses noise during engine start
- No plops when switching between standby and mute modes
- Slow offset change when switching from mute mode to operating mode (can be adjusted by an external capacitor)
- A fast mute function by discharging the external mute capacitor quickly

The following protection circuits are included to prevent the IC from being damaged:

- Thermal shutdown:

  At junction temperature T_{vj} > 170 °C, all power stages are switched off to prevent a further increase in temperature
- Soft thermal clipping:

  At junction temperature T_{vj} > 155 °C, the gain reduces as temperature increases, resulting in less output power and decreasing temperature and therefore no thermal shutdown (no break in the audio)
- Short-circuit protection:

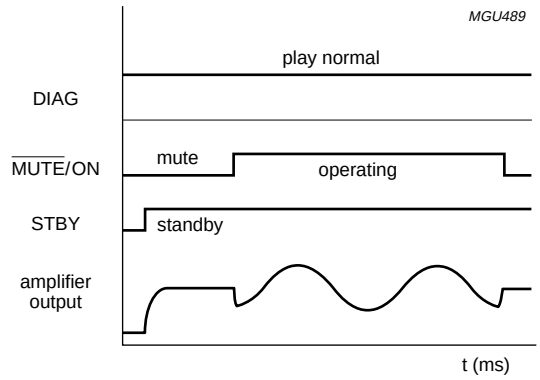
  If a short-circuit to ground or supply voltage occurs at one or more of the output pins, or across the load of one or more of the channels, the following action occurs to reduce power dissipation and case temperature (see Figs 5 and 6):
  - All amplifiers switch off for approximately 20 ms
  - After 20 ms the amplifiers switch on again
  - If the short-circuit persists, the amplifiers switch off for another 20 ms period and the action repeats
- ESD protection:
  - Human body model 2000 V
  - Machine model 200 V
- Protection against open ground pins and outputs short-circuited to supply ground (see Fig.30)
- All outputs protected are against open power supply pins and outputs short-circuited to power supply voltage (see Fig.31)
- With a reversed polarity power supply an external diode conducts and a fuse blows and therefore the reversed polarity voltage will not damage the device (see Fig.32).

7.1 Diagnostic facility

A diagnostic facility is available from the status of pin DIAG for the following conditions:

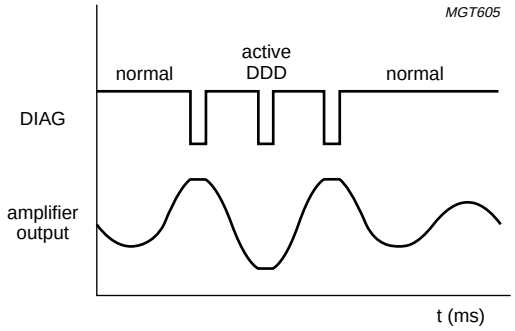
- In normal operation, the level on the DIAG pin is continuously HIGH (see Fig.3)
- When a temperature pre-warning occurs due to the junction temperature T_{vj} reaching 145 °C, the DIAG pin goes continuously LOW
- When there is distortion over 2.5% because of clipping, the DIAG pin has a pulsed output as shown in Fig.4
- When a short-circuit is detected, the short-circuit protection becomes active and DIAG goes continuously LOW for the period of the short-circuit (see Figs 5 and 6)
- With an extreme output offset, input leakage current causes a DC output offset voltage and results in power dissipation in the loudspeakers. Therefore, if the DC output offset voltage of a bridge is larger than 2 V, DIAG is pulled LOW to indicate an error condition.

The DIAG pin has an open-drain output to allow several devices to be tied together. An external pull-up resistor is needed.



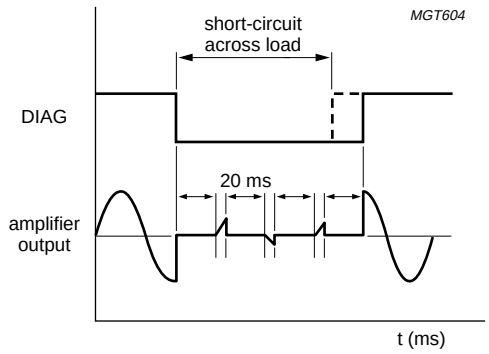
Pull-up resistor = 47 kΩ.

Fig.3 Diagnostic waveforms: standby, mute and operating mode sequence.



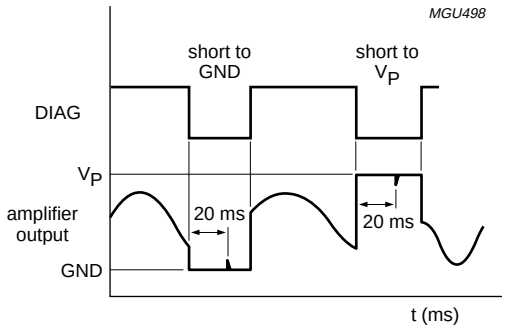
Pull-up resistor = 47 kΩ.

Fig.4 Diagnostic waveforms: dynamic distortion detection function.



Pull-up resistor = 47 kΩ.

Fig.5 Diagnostic waveforms: short-circuit across load.



Pull-up resistor = 47 kΩ.

Fig.6 Diagnostic waveforms: short-circuit to V_P pin or GND.

7.2 Diagnostic output (DIAG)

The internal circuit of the diagnostic open-drain output is shown in Fig.7.

A pull-up resistor is required if the diagnostic output is connected to a microcontroller. Figure 8 shows four possible solutions for fault diagnosis.

Figures 8a and 8b show simple configurations. The output offset diagnostic cannot trigger the microcontroller because of the 4-diode stack, only the temperature, short-circuit and dynamic distortion diagnostic will give an input LOW level for the microcontroller.

In Fig.8c, the diagnostic output is connected to an external level shifter. Now DIAG pin output can also generate an input LOW level for the microcontroller.

Assuming that a microcontroller HIGH input level must be equal to, or greater than 2 V, the following equations are used to calculate values for resistors R1 and R2:

$$V_{IN1} > 2\ V \text{ and } V_{IN1} = 5\ V - 4 \times V_d - R2 \times \left(\frac{5\ V - 4 \times V_d}{R1 + R2}\right)$$

where:

5 V is the pull-up supply voltage

V_d is the forward voltage of a diode (0.6 V)

R1 and R2 are the resistors in the level shifter.

Using both equations: $R1 > \frac{2 \times R2}{5\ V - 4 \times V_d - 2}$

thus R1 > 3.3 R2

Therefore, R1 can be 47 kΩ and R2 can be 10 kΩ.

The level shifter shown in Fig.8d is used as a 2-bit analog-to-digital converter.

With reference to Figs 7 and 8c, the truth table in Table 1 can be made:

Table 1 Truth table.

HIGH TEMPERATURE OR SHORT-CIRCUIT OR DDD	OFFSET	IN1	IN2
no	no	1	1
no	yes	0	1
yes	don't care	0	0

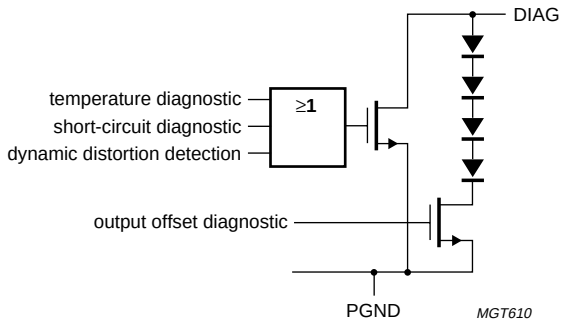
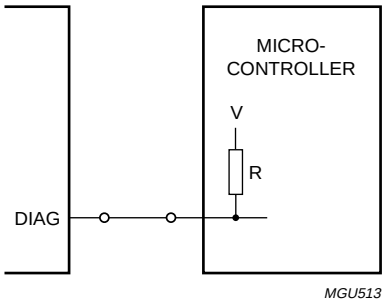
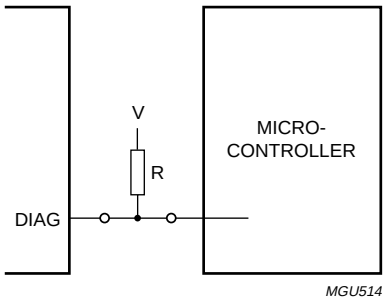


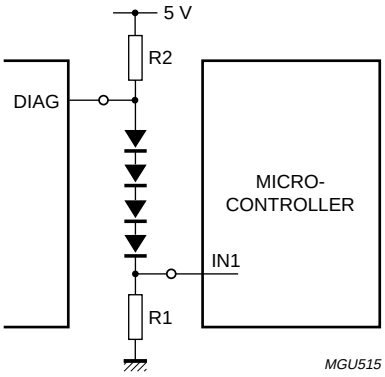
Fig.7 Internal circuit diagnostic output pin DIAG.



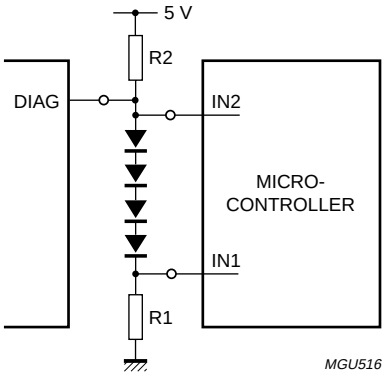
a. Internal pull-up.



b. External pull-up.



c. Level shifter.



d. Two-pin diagnostics.

Fig.8 Connecting the DIAG output to a microcontroller input.

7.3 Mute timer and single-pin mute control

The transition time from mute mode to operating mode can be used to hide plops that occur during switching. This transition time is determined by the value of the external capacitor at the $\overline{\text{MUTE}}$/ON input (see Fig.33). To guarantee the mute suppression, the resistor value may not be more than 15 kΩ. The switching can be controlled by a transistor switch with an open-drain output or a voltage output with a minimum high level of 5.5 V.

When controlling with an open-drain output, the high voltage level also must be at least 5.5 V and should not be clamped on a lower value by the ESD diode of the microcontroller. If the minimum high voltage cannot be guaranteed, an external open-drain transistor or switch to ground can be used. Charging of the external capacitor at the $\overline{\text{MUTE}}$/ON input is done by an internal current source.

If muting is performed by the microcontroller, the mute connection to the microcontroller can be omitted. The mute on and off transitions during start-up and switch-off are controlled by an internal push-pull current source and the external capacitor at pin 8 ($\overline{\text{MUTE}}$/ON).

Fast mute can be achieved by quickly discharging the mute capacitor by means of an open-drain transistor without a series resistor.

7.4 Output power

EIAJ power is a power rating which indicates the maximum possible output power of a specific application at a nominal supply voltage. The power losses caused by PCB layout, copper area, connector block, coil, loudspeaker wires, etc. depend on the applications.

Therefore, the EIAJ power is defined and measured at the pins of the IC using the following test conditions:

- The supply voltage is 14.4 V measured on the pins of the TDA8591J
- All channels are loaded with 4 Ω and are driven simultaneously
- The input signal is a continuous (no burst) square wave:

  V = 1 V (RMS); f = 1 kHz
- RMS output power is measured immediately at the start (cold heatsink) and after 1 minute of operation. The mean value is the rated EIAJ power.

To have optimum output power performance, the external heatsink should be chosen carefully. A small heatsink causes a high junction temperature, resulting in an increase of the drain-source on-state resistance (R_{DSon}) of the power amplifiers and a decrease of the maximum output power.

The reason for using a square wave input signal for EIAJ power measurement is illustrated in Fig.9.

Figure 9a shows a square wave signal with

$$\text{slew rate} = \frac{V_{top}}{t_r}$$

Assuming this square wave is the output signal of an amplifier, the EIAJ output power is given by

$$P_{EIAJ} = \frac{V_{top}^{2}}{R_L} \times \frac{1 - \left(\frac{8}{3}\right) \times V_{top} \times f}{\text{slew rate}}$$

where:

R_L = load resistor in Ω

V_{top} = maximum voltage across the load in V

f = frequency of the square wave in Hz

t_r = rise time of the slope in s.

A sine wave has a lower slew rate than a square wave as shown in Fig.9b, therefore EIAJ power measurement with a sine wave will give a lower power value. The maximum slew rate of a sine wave output signal is given by

$$\frac{\delta U_{out}}{\delta t\ \text{max}} = \frac{\delta(A \times \sin(2\pi f \times t))}{\delta t\ \text{max}} = 2\pi f \times A$$

where:

A = amplitude of the output sinewave in V

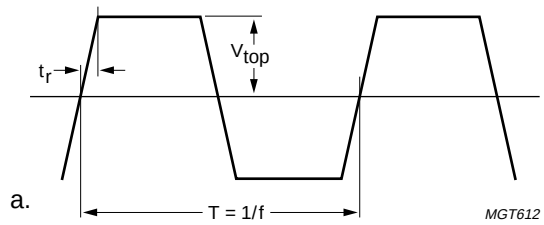
f = frequency of the output sinewave in Hz.

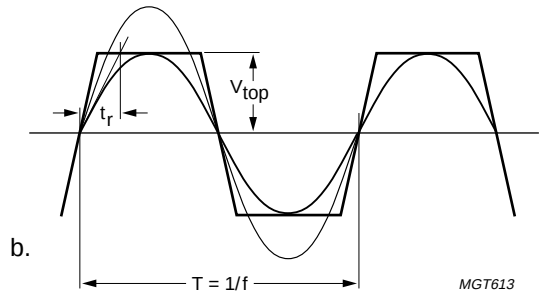
For a non-clipping sinewave output with amplitude A = 13 V and frequency f = 1 kHz, the slew rate is

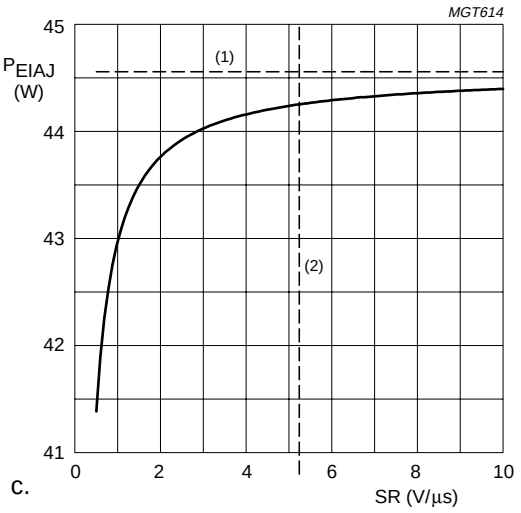
$$\frac{\delta U_{out}}{\delta t\ \text{max}} = 82^{3}\ \text{V/s}$$

A faster slew rate can be obtained by increasing the amplitude: for an amplitude of 28 V, the slew rate will increase to 1.8^{5} V/s. A supply voltage of V_P = 14.4 V will result in a clipped output with a shape similar to a square wave but with a slower slew rate.

Figure 9c shows the dependency of P_{EIAJ} on slew rate. Using a square wave input signal, the EIAJ output power is determined by the drop voltage and bandwidth of the output stage.







(1) $P_{EIAJ(max)}$ (infinite slew rate).
(2) Maximum slew rate of TDA8591J.

Fig.9 Comparison of sine wave and square wave RMS powers.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		not operating	–1	+45	V
		with load dump protection (see Fig.10)	–	45	V
V_{DIAG}	voltage on pin DIAG		–	45	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	6	A
V_{sc}	AC and DC short-circuit voltage	short-circuit of output pins across loads and to ground or supply	–	18	V
V_{rp}	reverse polarity voltage	$t \leq 1$ ms	–	6	V
P_{tot}	total power dissipation	T_{case} = 70 °C	–	80	W
T_{vj}	virtual junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{esd}	electrostatic handling voltage	note 1	2000	–	V
		note 2	200	–	V

Notes

1. Human body model: C = 100 pF; R_S = 1500 Ω; all pins have passed all tests to 2500 V to guarantee 2000 V, according to *"General Quality Specification SNW-FQ-611D"*, class II, except pin GND, which passed 2200 V, class Ia.
2. Machine model: C = 200 pF; R_S = 10 Ω; L = 0.75 mH.

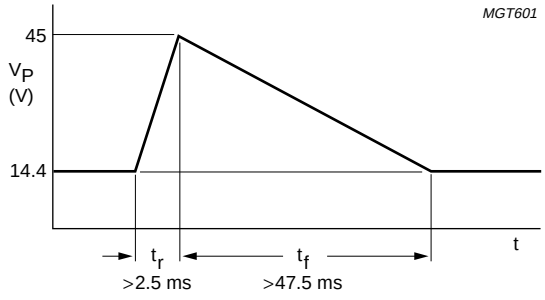


Fig.10 Load dump pulse definition.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	see Fig.11	1	K/W

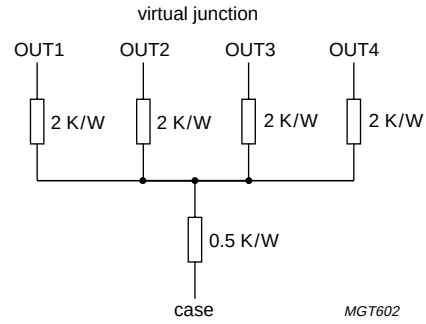


Fig.11 Equivalent thermal resistance network.

10 QUALITY SPECIFICATION

Quality according to *"SNW-FQ-611E"*.

11 DC CHARACTERISTICS

T_{amb} = 25 °C; R_L = ∞; $V_P = V_{P1} = V_{P2} = V_{P3}$ = 14.4 V; measured in the circuit of Fig.29; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage		8.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current		120	200	290	mA
I_{stb}	standby current		–	2	50	µA
V_O	DC output voltage		–	7.2	–	V
$V_{P(mute)}$	low supply voltage mute	operating to mute mode	6.0	7.0	8.0	V
		mute to operating mode	6.3	7.0	8.5	V
$V_{P(mute)(hys)}$	low supply voltage mute hysteresis		–	0.4	–	V
$\lvert V_{OO} \rvert$	output offset voltage	mute mode; $V_{\overline{MUTE}/ON}$ = 0 V	–	0	30	mV
		operating mode; $V_{\overline{MUTE}/ON}$ = 5 V	–	0	60	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
STBY and $\overline{\text{MUTE}}$/ON inputs (see Table 2)						
V_{STBY}	control voltage on pin STBY	standby mode	0	–	0.8	V
$V_{STBY(hys)}$	voltage hysteresis on pin STBY		–	0.2	–	V
$V_{\overline{\text{MUTE}}/ON}$	voltage on pin $\overline{\text{MUTE}}$/ON	mute mode; $V_{STBY} > 2.5$ V	–	–	0.8	V
		operating mode; $V_{STBY} > 2.5$ V; note 1	5.5	–	V_P	V
I_{STBY}	STBY pin current	$V_{STBY} = 5$ V	–	–	80	µA
$\lvert I_{\overline{\text{MUTE}}/ON} \rvert$	$\overline{\text{MUTE}}$/ON pin current	$V_{\overline{\text{MUTE}}/ON} = 5.5$ V	–	25	–	µA
DIAG output (see Figs 3 to 6)						
V_{DIAG}	diagnostic output voltage	$I_{DIAG(sink)} = 250$ µA DDD, protection circuits and temperature pre-warning active	– 	0.3 	0.8 	V
		offset diagnostic active	2.0	2.8	3.2	V
I_L	leakage current	$V_{DIAG} = 14.4$ V	–	–	1	µA
THD	total harmonic distortion at clip detection	$V_{DIAG} < 0.8$ V	–	1.5	–	%
$\lvert V_{OO(det)} \rvert$	output offset voltage detection; note 2	$2.0 < V_{DIAG} < 3.2$ V	2.5	4.5	6.5	V
T_{vj}	virtual junction temperature	temperature pre-warning; $V_{DIAG} < 0.8$ V	135	145	–	°C
		soft thermal clipping; $G_V = -3$ to -23 dB	–	155	–	°C
		temperature shut-down	–	170	–	°C

Notes

1. With open $\overline{\text{MUTE}}$/ON pin, the TDA8591J will switch to operating mode (see Section 7.3)
2. $V_{OO(det)}$ is the offset voltage across the load. Pin OFFCAP should never be left open-circuit. If pin OFFCAP is connected to one of the PGND pins, the offset detection is switched off (see Section 14.4).

Table 2 Mode selection

STBY	$\overline{\text{MUTE}}$/ON	AMPLIFIER MODE
0	don't care	standby (off)
1	0	mute (DC settled)
1	1	operating

12 AC CHARACTERISTICS

$V_P = V_{P1} = V_{P2} = V_{P3} = 14.4$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^oC$; measured in the circuit of Fig.29; unless otherwise specified.

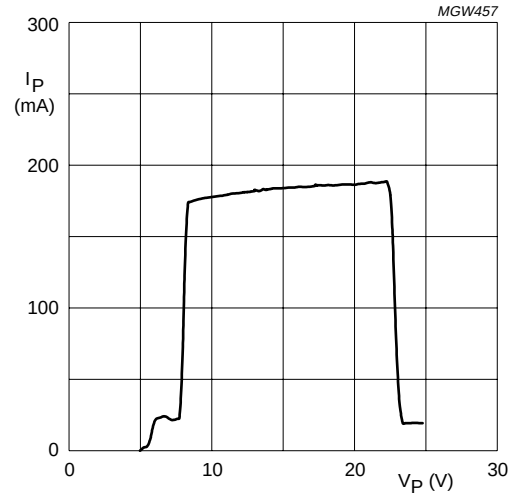
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD + N = 0.5 %				
		$R_L = 4\ \Omega$	20	22	–	W
		$R_L = 2\ \Omega$	–	34	–	W
		THD + N = 1 %; $R_L = 2\ \Omega$	–	35	–	W
		THD + N = 10 %				
		$R_L = 4\ \Omega$	27	28	–	W
		$R_L = 2\ \Omega$	–	47	–	W
		EIAJ values				
		$R_L = 4\ \Omega$	41.5	44		W
		$R_L = 2\ \Omega$	–	75	–	W
G_v	voltage gain	V_i = 40 mV (RMS)	25	26	27	dB
THD + N	total harmonic distortion plus noise	P_o = 1 W; f = 1 kHz	–	0.03	0.1	%
		P_o = 10 W; f = 10 kHz	–	0.2	–	%
α_{cs}	channel separation	V_i = 40 mV (RMS); $R_S = 0\ \Omega$	56	68	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	1	dB
$V_{n(o)}$	noise output voltage	$R_S = 0\ \Omega$; note 1				
		operating mode	–	70	110	μV
		mute mode	–	16	–	μV
$V_{o(mute)}$	output voltage in mute mode	mute mode; V_i = 1 V (RMS)	–	16	30	μV
SVRR	supply voltage ripple rejection	V_{ripple} = 2 V (p-p); mute or operating mode; $R_S = 0\ \Omega$	54	68	–	dB
Z_i	input impedance	$V_i \leq 3$ V (RMS)	60	70	–	kΩ
CMRR	common mode rejection ratio	$R_S = 0\ \Omega$; V_{cm} = 0.35 V (RMS)	–	70	–	dB
B_P	power bandwidth	THD + N = 0.5%; P_o = –1 dB with respect to 17 W	–	20 to 20000	–	Hz
$f_{ro(l)}$	low frequency roll-off	at –1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	at –1 dB	150	300	–	kHz

Notes

1. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz.
2. The frequency response is fixed with external components.

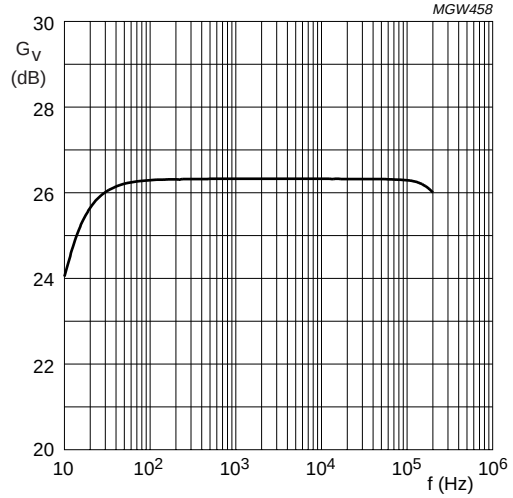
12.1 Performance curves

Conditions for Figs 12 to 28 unless otherwise specified are: V_P = 14.4 V; R_L = 4 Ω: f = 1 kHz; 80 kHz filter.



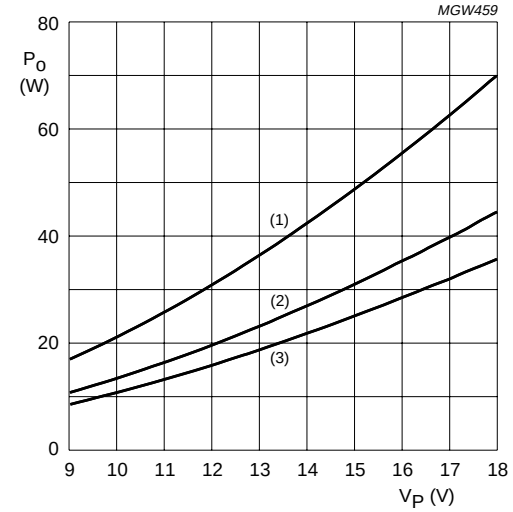
$R_L = \infty$.

Fig.12 Supply current as a function of supply voltage.



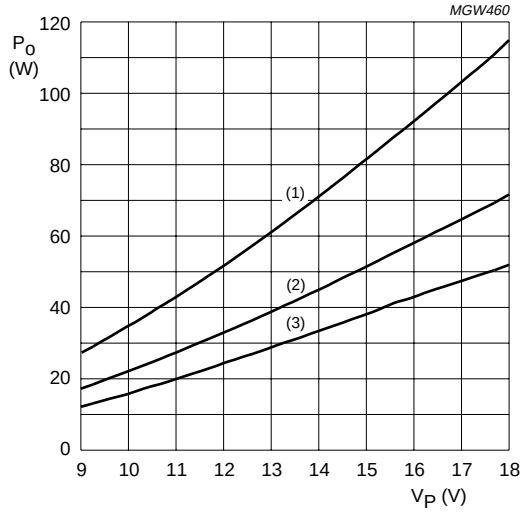
V_i = 10 mV.

Fig.13 Voltage gain as a function of frequency.



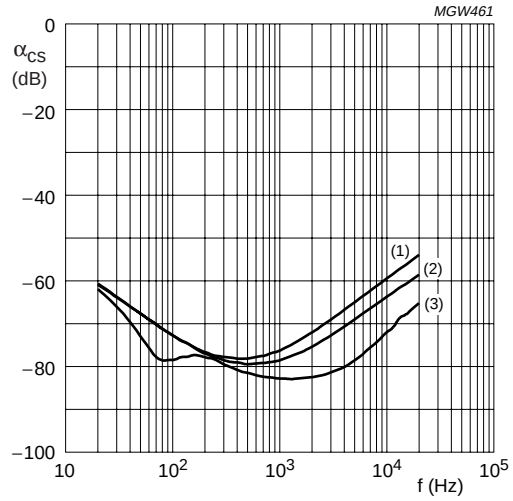
One channel driven.
(1) EIAJ values.
(2) THD + N = 10%.
(3) THD + N = 1%.

Fig.14 Output power as a function of supply voltage; R_L = 4 Ω.



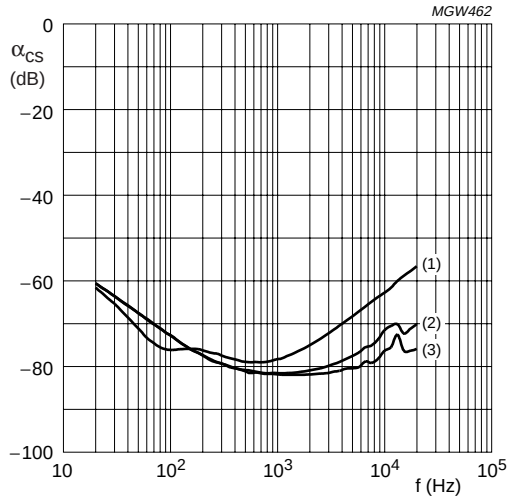
One channel driven.
(1) EIAJ values.
(2) THD + N = 10%.
(3) THD + N = 1%.

Fig.15 Output power as a function of supply voltage; R_L = 2 Ω.



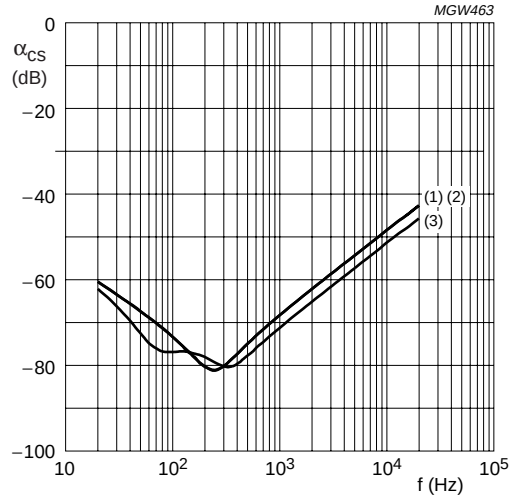
P_o = 1 W.
(1) Separation between channels 1 and 3.
(2) Separation between channels 1 and 4.
(3) Separation between channels 1 and 2.

Fig.16 Channel separation as a function of frequency; channel 1 driven.



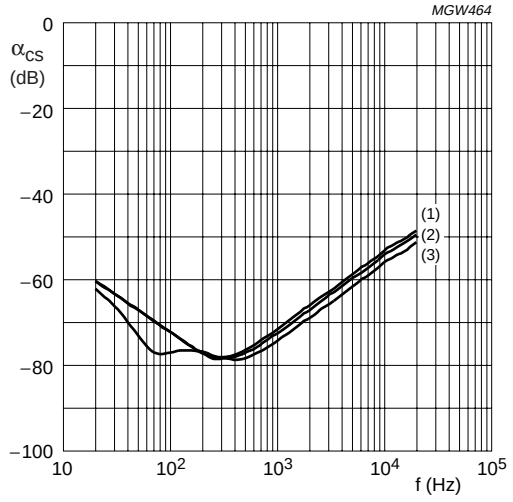
P_o = 1 W.
(1) Separation between channels 2 and 1.
(2) Separation between channels 2 and 3.
(3) Separation between channels 2 and 4.

Fig.17 Channel separation as a function of frequency; channel 2 driven.



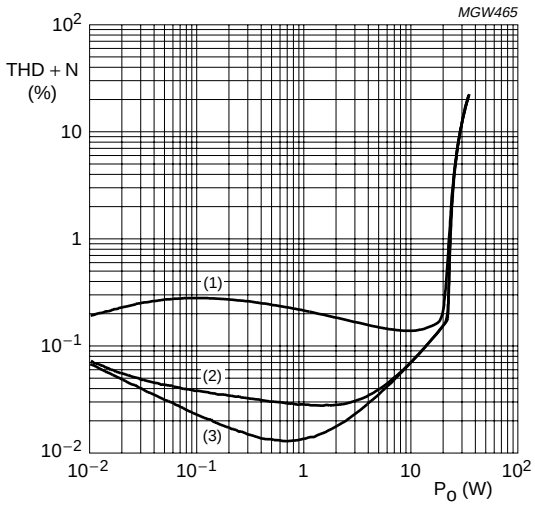
P_o = 1 W.
(1) Separation between channels 3 and 1.
(2) Separation between channels 3 and 2.
(3) Separation between channels 3 and 4.

Fig.18 Channel separation as a function of frequency; channel 3 driven.



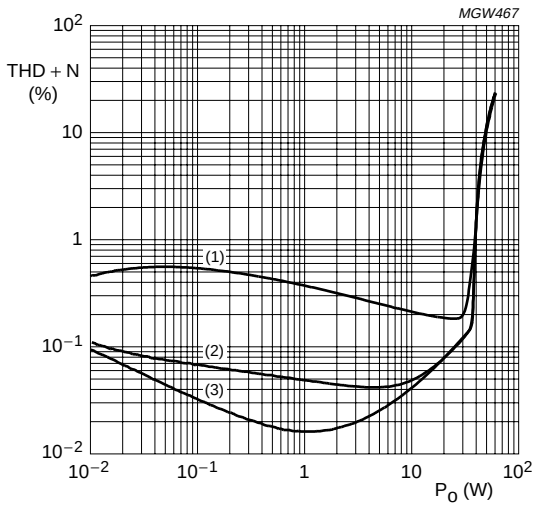
P_o = 1 W.
(1) Separation between channels 4 and 1.
(2) Separation between channels 4 and 2.
(3) Separation between channels 4 and 3.

Fig.19 Channel separation as a function of frequency; channel 4 driven.



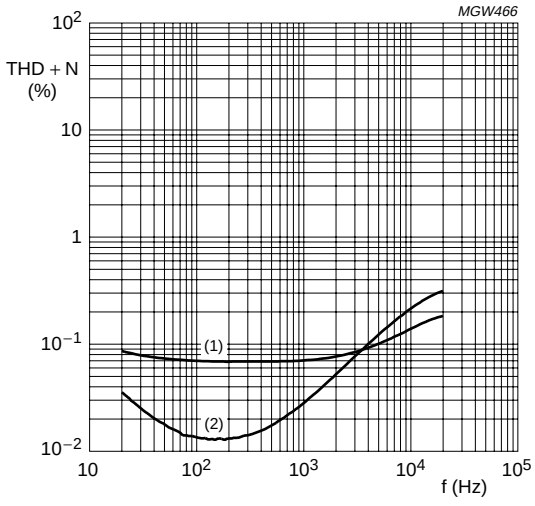
(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.20 Total harmonic distortion plus noise as a function of output power; R_L = 4 Ω.



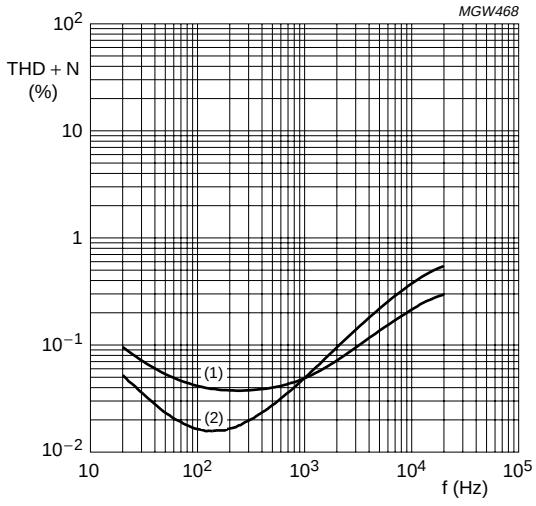
(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.21 Total harmonic distortion plus noise as a function of output power; R_L = 2 Ω.



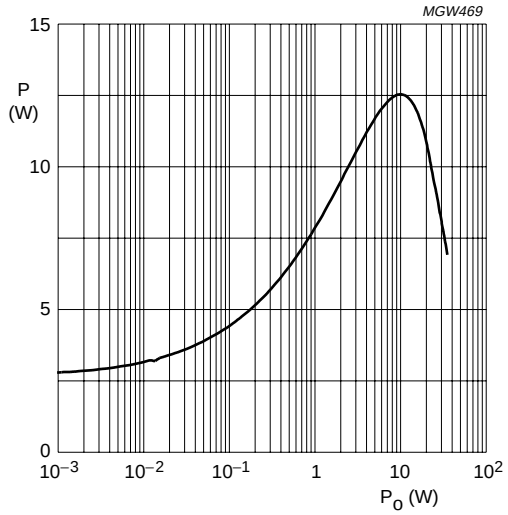
(1) P_o = 1 W.
(2) P_o = 10 W.

Fig.22 Total harmonic distortion plus noise as a function of frequency; R_L = 4 Ω.



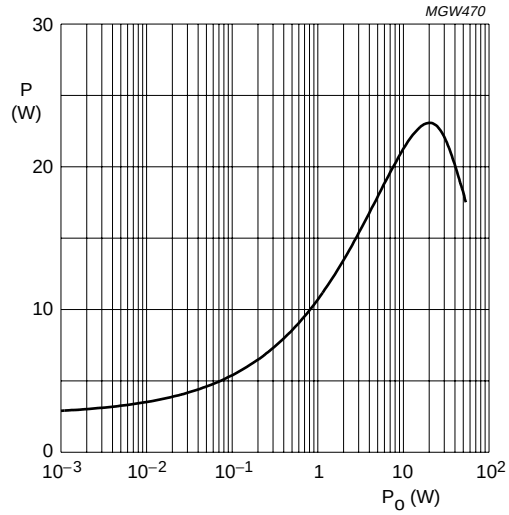
(1) P_o = 1 W.
(2) P_o = 10 W.

Fig.23 Total harmonic distortion plus noise as a function of frequency; R_L = 2 Ω.



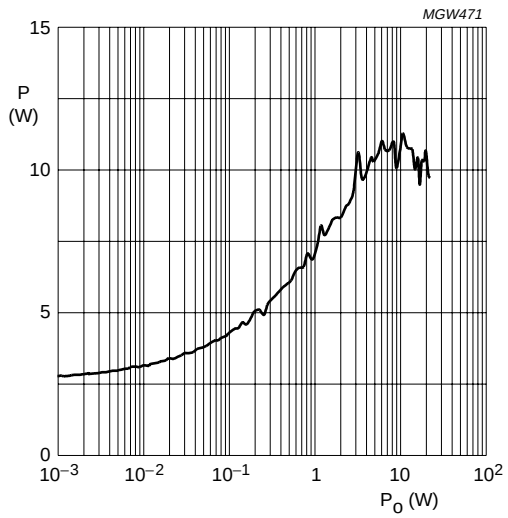
Sine wave input; one channel driven.

Fig.24 Power dissipation as a function of output power; R_L = 4 Ω.



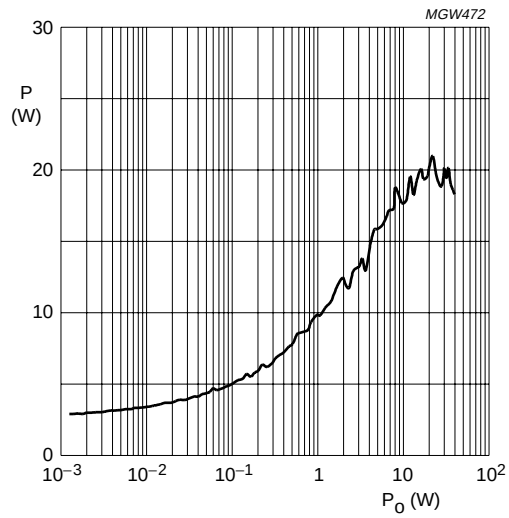
Sine wave input; one channel driven.

Fig.25 Power dissipation as a function of output power; R_L = 2 Ω.



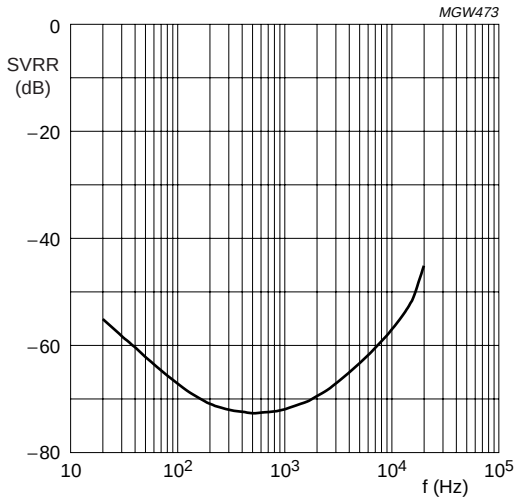
IEC60268 filtered noise; one channel driven.

Fig.26 Power dissipation as a function of output power; R_L = 4 Ω.



IEC60268 filtered noise; one channel driven.

Fig.27 Power dissipation as a function of output power; R_L = 2 Ω.



V_{ripple} = 2 V (p-p).

Fig.28 Supply voltage ripple rejection as a function of frequency.

13 TEST INFORMATION

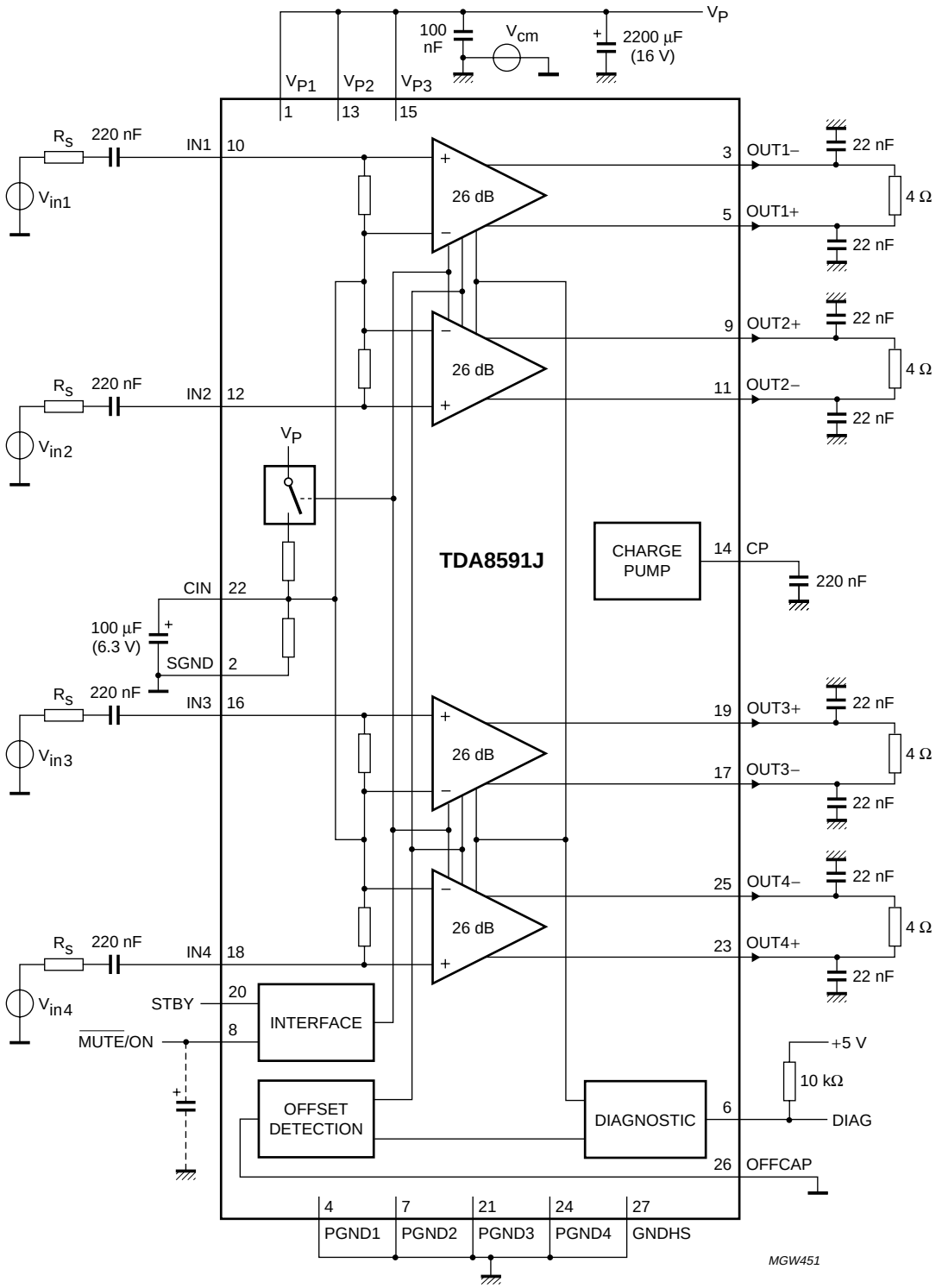
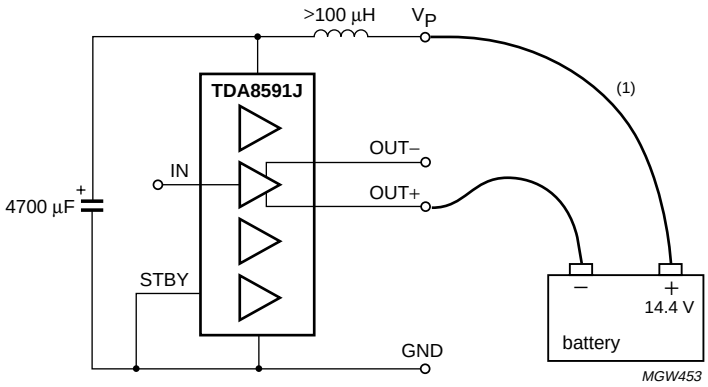


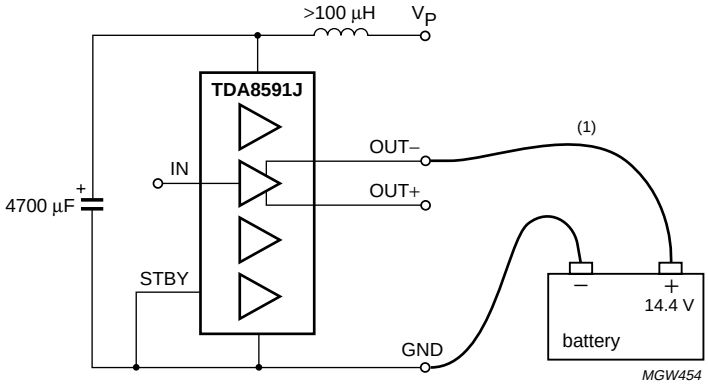
Fig.29 Test circuit.

13.1 Protection circuit testing



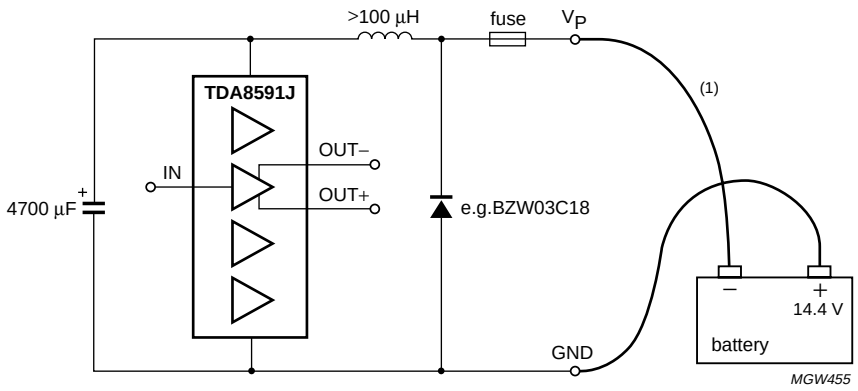
One channel output shown.
At the start of the test, the 4700 µF capacitor should be discharged.
The amplifier is in standby during test.
(1) Cable length is 1 metre, cable diameter is 1.5 mm.

Fig.30 Open ground pin test set-up.



One channel output shown.
At the start of the test, the 4700 µF capacitor should be discharged.
The amplifier is in standby during test.
(1) Cable length is 1 metre, cable diameter is 1.5 mm.

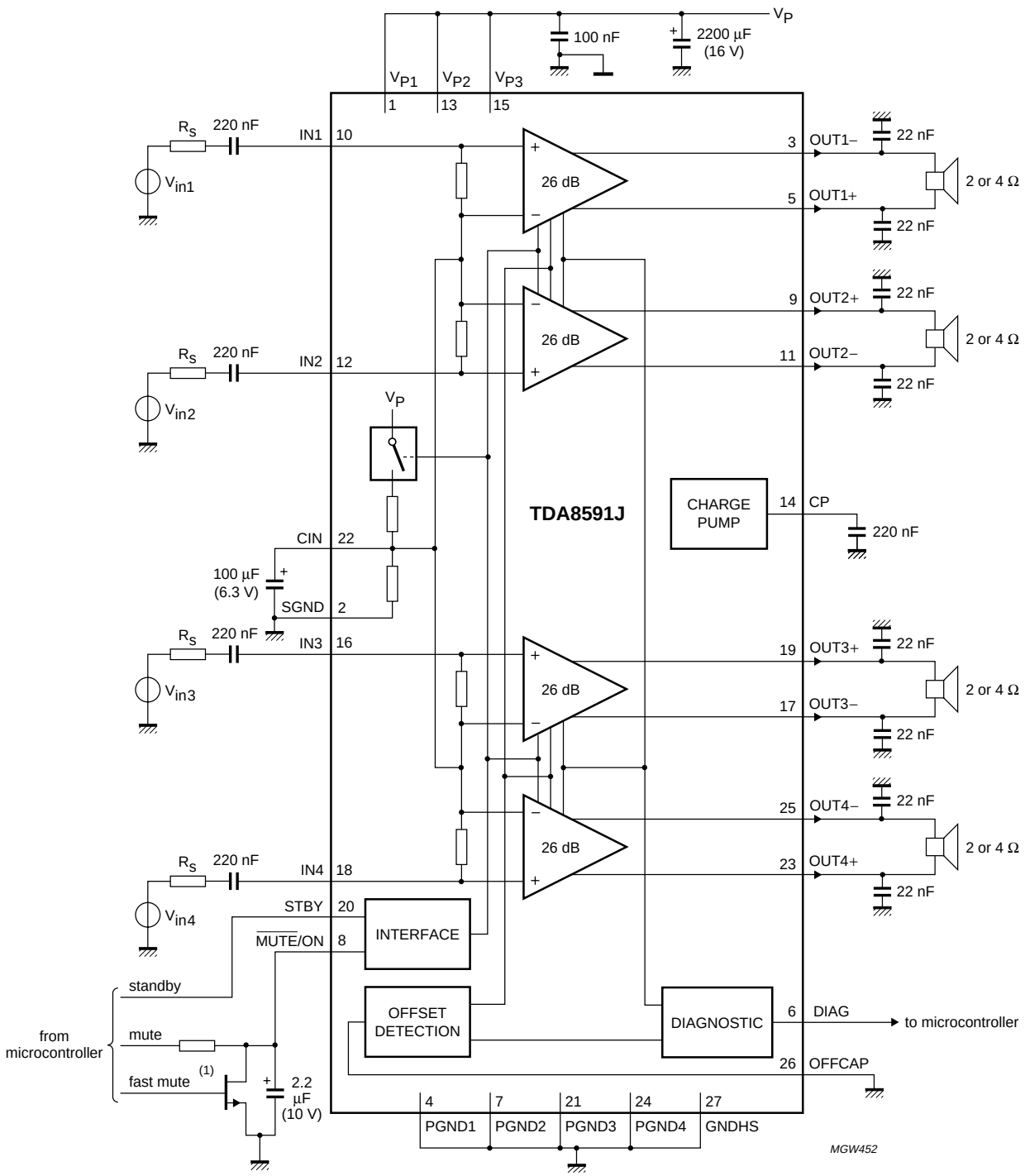
Fig.31 Open power supply (pin V_P) test set-up.



(1) Cable length is 1 metre, cable diameter is 1.5 mm.

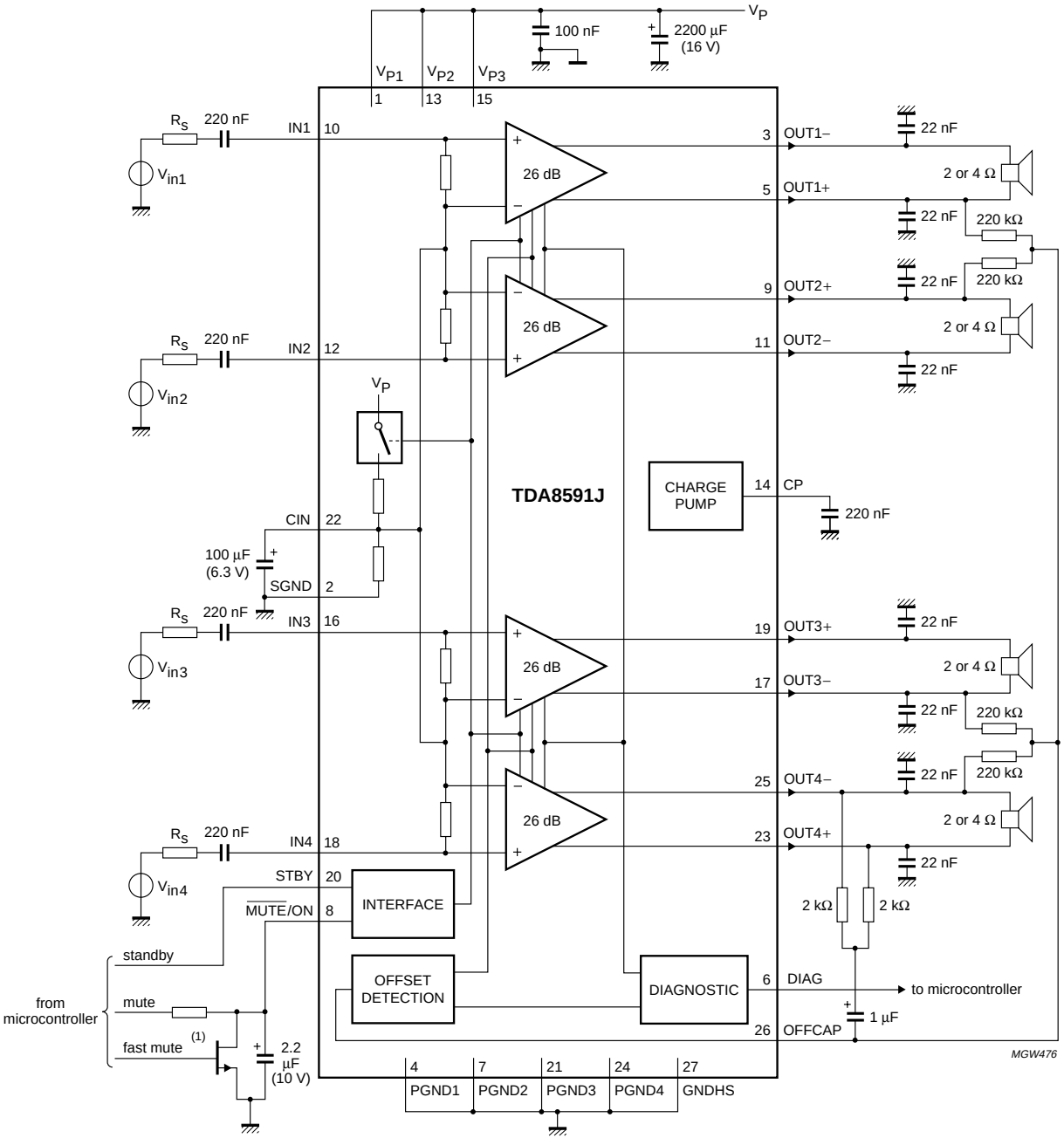
Fig.32 Reversed polarity power supply test set-up.

14 APPLICATION INFORMATION



(1) Not needed with single-pin mute control.

Fig.33 Quad BTL application without offset detection circuit.



(1) Not needed with single-pin mute control.

Fig.34 Quad BTL application with offset detection circuit.

14.1 Special attention for SMD input capacitors

When SMD capacitors are used as input capacitors, low frequency noise can occur due to stress on the PCB. The SMD capacitors can operate like small microphones with sensitivity of $\frac{1}{f}$. Special attention should be paid to this issue when selecting SMD capacitors at the four inputs (MKT capacitors are recommended).

14.2 Capacitors on outputs

The TDA8591J is optimized for a capacitor of 22 nF from each output to ground for RF immunity and ESD. These capacitors can be replaced by the capacitors on the connector block.

14.3 EMC precautions

The TDA8591J has an all N-type DMOS output stage. The main advantage of having the same type of power transistors in the output stage is symmetrical behaviour for positive and negative signals (sound quality).

A charge pump (DC to DC converter with capacitors only) is used to generate a voltage above the battery voltage to drive the high-side power. The clock frequency of the charge pump (2.9 MHz) is chosen above the AM frequency band. To prevent possible crosstalk in the FM frequency band, a SIL pad can be used between the rear of the TDA8591J and the heatsink. This SIL pad is an electrical isolator and thermal conductor. It is advisable to connect the power supply lines of the TDA8591J directly to the power supply on the printed circuit board of the radio, so that a one-point earth bonding with the tuner supply is achieved.

The external capacitor of the charge pump (connected to pin CP) filters and buffers the voltage generated internally. The loop area of the capacitor connected to pins CP and PGND2 should be kept as small as possible. For optimum performance the capacitor used should have a good frequency performance, for example an SMD ceramic capacitor. See Figs 35 and 36 for a good PCB layout.

14.4 Offset detection

As shown in Fig.34, to obtain the DC offset information, an output from each bridge is summed and filtered through external 220 kΩ resistors and a 1 μF capacitor at pin OFFCAP. The low frequency roll-off can be chosen with the resistor/capacitor combination. Because of the random phase of the DC offset voltage, the capacitor on pin OFFCAP should not be a conventional electrolytic capacitor as leakage current in this capacitor would cause a shift in low frequency roll-off because of no pre-biasing.

If the offset detection is not used, pin OFFCAP can be connected to ground, the external components (resistors of 220 kΩ and 2 kΩ and the capacitor of 1μF) are not needed and the circuit is as shown in Fig.33.

14.5 Channel selection

The following recommendation for a four channel application is given on the basis of the results of the channel separation measurements and the dissipation spread within the package:

Front-left = OUT1

Rear-left = OUT2

Rear-right = OUT3

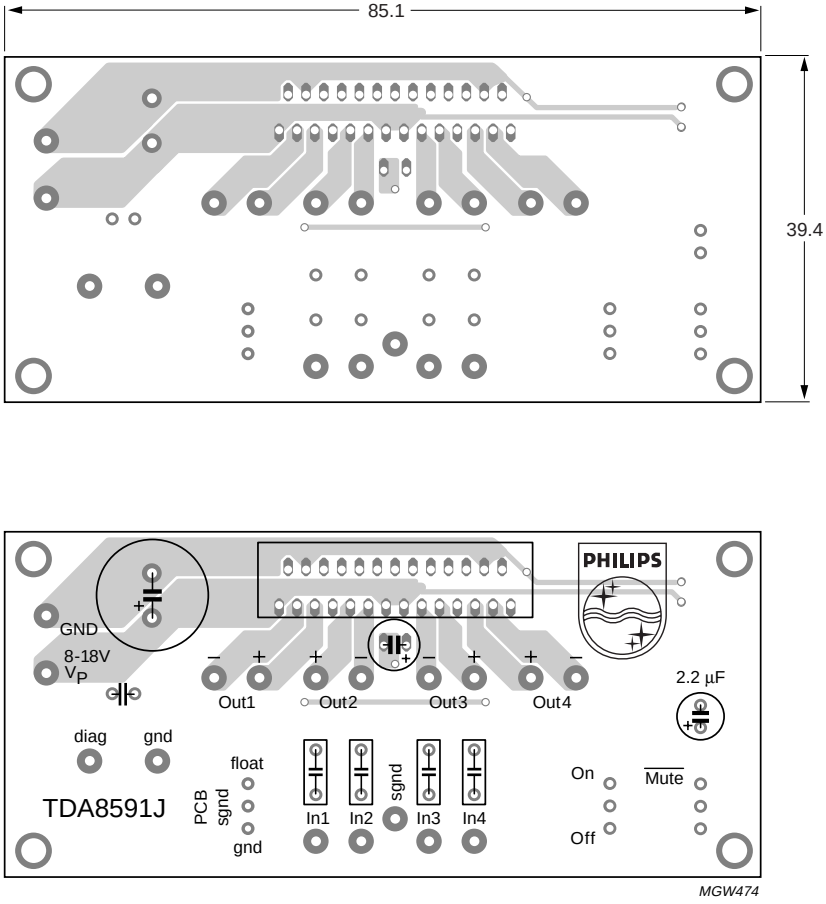
Front-right = OUT4.

14.6 Detection of short-circuits

Table 3 Detection of short-circuits in standby, mute and operating modes.

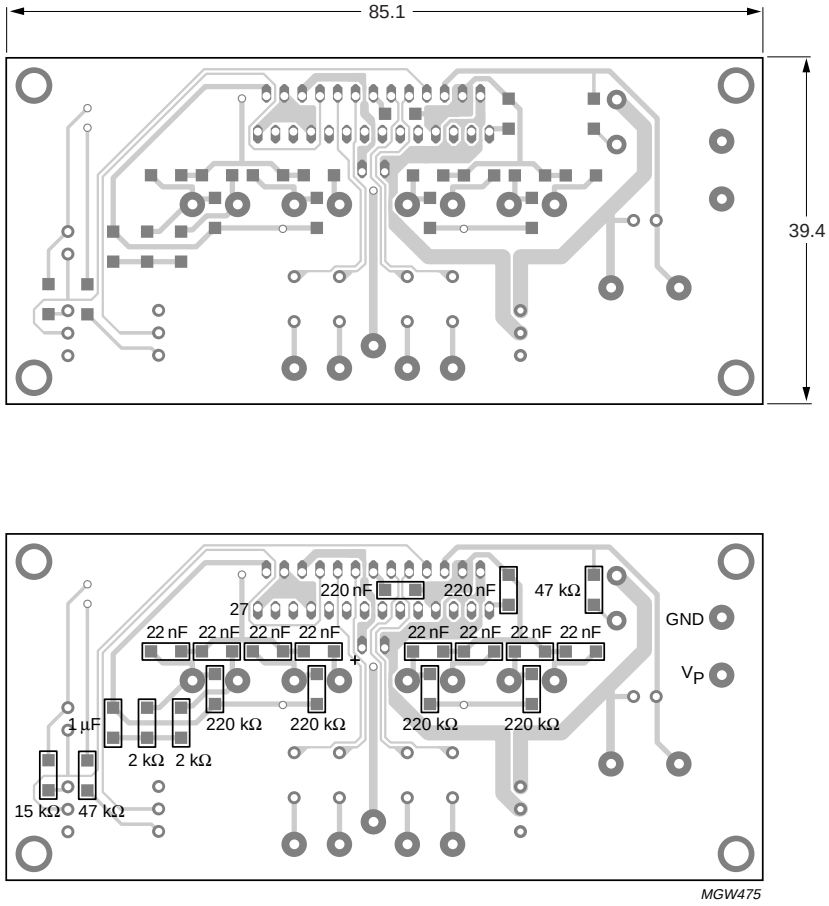
AMPLIFIER MODE	SHORT-CIRCUIT ACROSS LOAD	SHORT-CIRCUIT TO SUPPLY OR GROUND
Standby	no diagnosis	no diagnosis
Mute (no output signal)	the value of short-circuit that activates diagnosis and protection depends on the output offset voltage	no diagnosis and no active protection if short-circuit >100 Ω
Operating (output signal present)	diagnosis and active protection if short-circuit <0.4 Ω	no diagnosis and no active protection if short-circuit >100 Ω

14.7 PCB layout



Dimensions in mm.

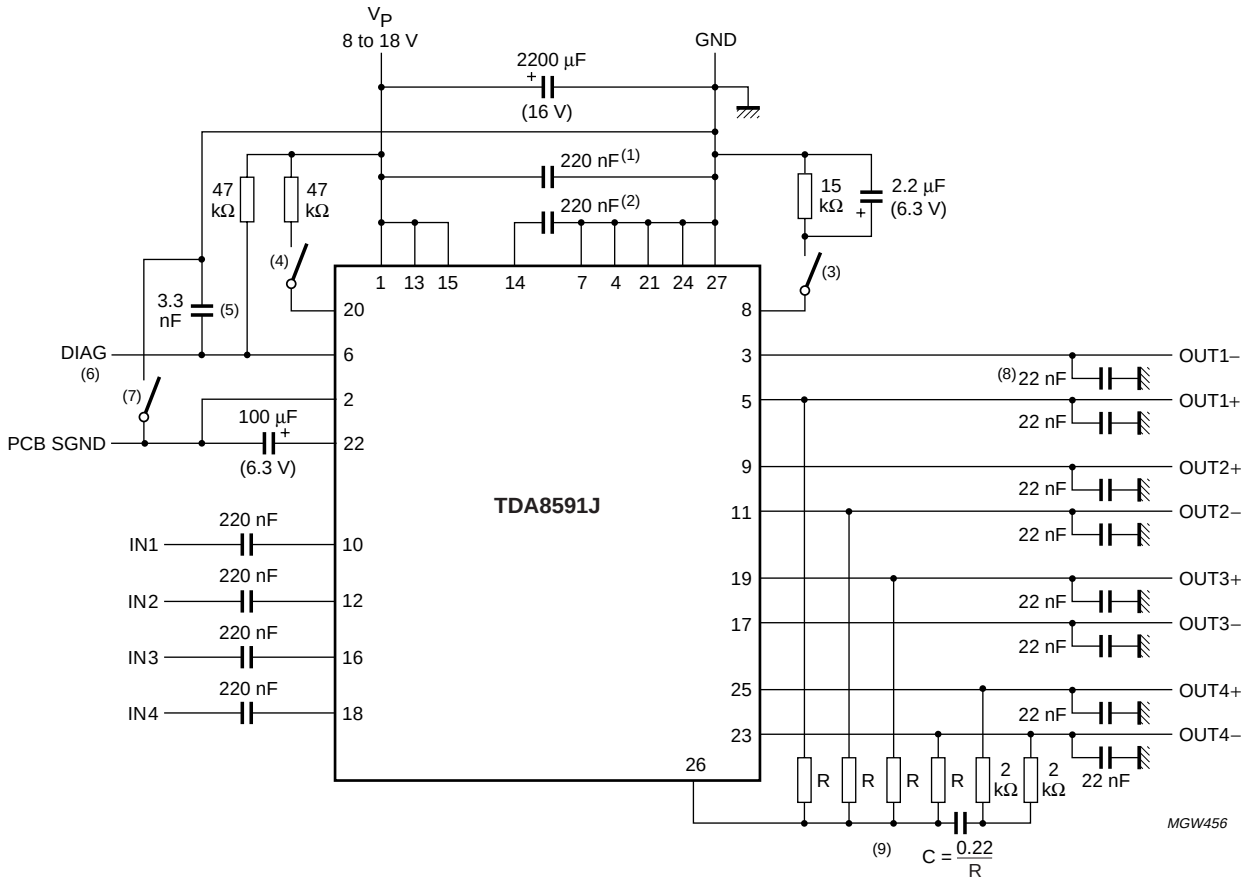
Fig.35 PCB layout (component side).



Dimensions in mm.

Fig.36 PCB layout (soldering side).

14.8 PCB design advice



(1) Power supply high frequency capacitor to be mounted close to the IC. An SMD component is recommended.

(2) Charge pump capacitor to be mounted close to the IC between pins 14 and 7.

(3) Switch closed is the mute mode.

(4) Switch open is the standby mode.

(5) A 3.3 nF capacitor has been added to provide a smooth offset detection diagnostic.

(6) Diagnostic output is less than 0.8 V when DDD or temperature pre-warning or protection circuits are activated.

(7) Signal ground switch is closed if the source is floating. Avoid ground loops in the input signal path. Keep inputs and signal ground close together.

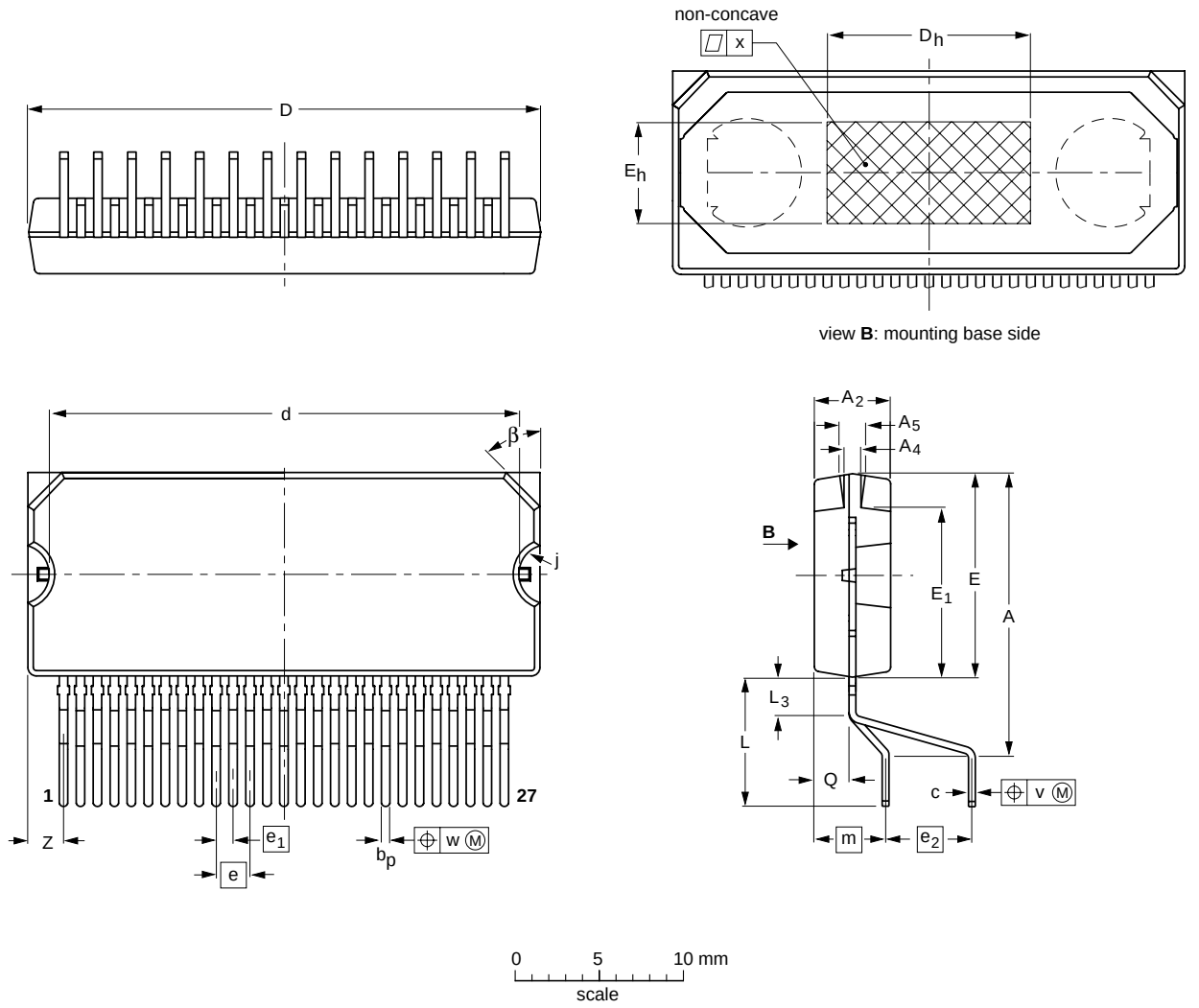
(8) The 22 nF capacitors on the outputs can be replaced by the capacitor on the connector block to ground, where it is often used for RF immunity and ESD suppression.

(9) Offset detection: if R = 100 kΩ then C = 2.2 nF; if R = 220 kΩ then C = 1 µF. An electrolytic capacitor is not allowed because of the random phase of the DC offset.

Fig.37 PCB design advice.

15 PACKAGE OUTLINE

DBS27P: plastic DIL-bent-SIL power package; 27 leads (lead length 7.7 mm) **SOT521-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	j	L	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	17.0 15.5	4.6 4.3	1.15 0.85	1.65 1.35	0.60 0.45	0.5 0.3	30.4 29.9	28.0 27.5	12	12.2 11.8	2.0	1.0	4.0	6	10.15 9.85	1.85 1.65	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	2.4 1.8

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT521-1						99-01-05

16 SOLDERING

16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

16.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

17 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

18 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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